FAST CMOS CCD DRIVER

FEATURES

- Operating Range.....4.5V ≤ (V_{DD} – V_{SS}) ≤ 12V
- TTL/CMOS-Compatible Inputs
- Low Delay Time .....15 ns Typ
- Rise and Fall Times .....2200 pF Load, 25 ns Typ
- Peak Output Current 3A
- Output Can Be Floated Below Digital Return
- Level Shifting for Split-Supply Operation
- Guaranteed Skew
- Complementary Outputs
- 10 MHz Operation With Adequate Heat Sink
- Drives 1000 pF at 4 MHz, in CerDIP With No External Heat Sink (10V V_{DD} – V_{SS})
- Low Output Impedance.....5Ω Max
- Low Quiescent Current.....5 mA Max

APPLICATIONS

- CCD Driver
- MOSFET Driver
- Laser Diode Driver
- Differential Line Driver
- PIN Diode Driver
- Level Shifting Driver

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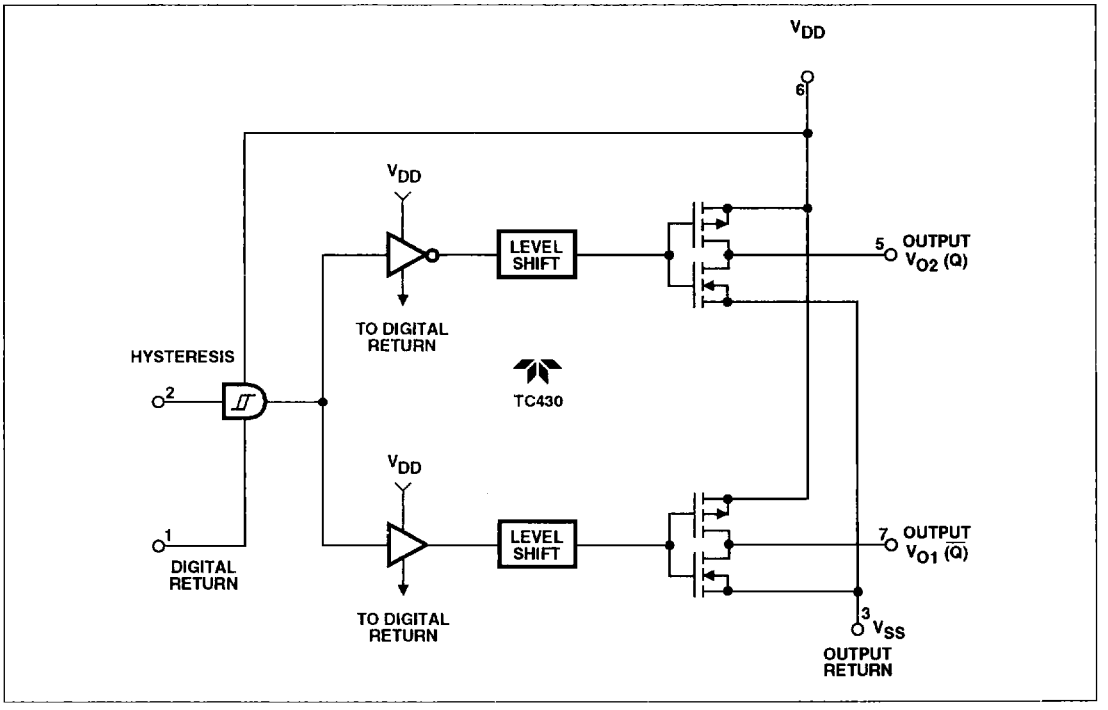
FUNCTIONAL DIAGRAM



1020-1

TC430

GENERAL DESCRIPTION

The TC430 is a super-fast CMOS power driver for driving CCDs and other loads. The TC430 operates at frequencies to 10 MHz and drives loads greater than 2200 pF. Peak current output is 3A.

The input is TTL/CMOS compatible. Digital return and output return can be at different voltages, allowing operation with output swings between positive and negative supplies without sacrificing AC performance when driven from TTL. The ability to swing negative is important when driving CCD devices.

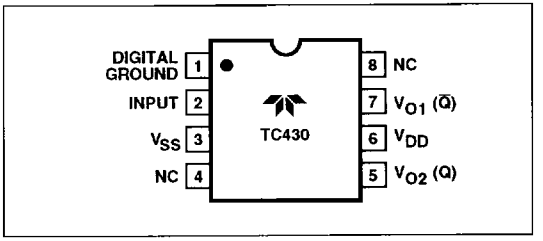
The output stages have been designed so the rising edge of one output crosses the 50% point of the transition within 5 ns of the other. This makes the TC430 ideal for driving CCDs and achieving high contrast images.

CMOS construction achieves low quiescent power (less than 5 mA at 15V and 25°C) and low input current requirements. This device requires fewer external components than bipolar devices like the DS0026 which need external speed-up capacitors.

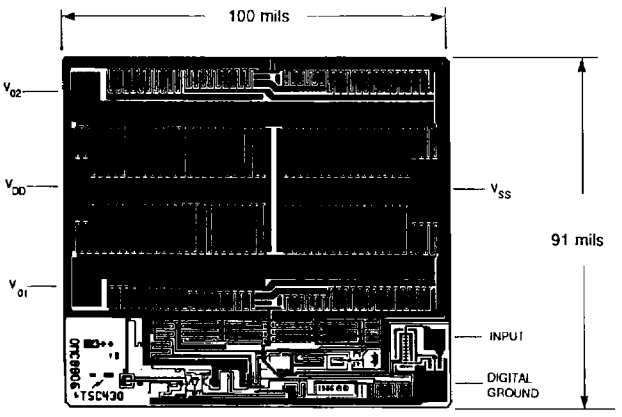
ORDERING INFORMATION

Part No.	Package	Temperature Range
TC430CPA	8-Pin Plastic	0°C to +70°C
TC430IJA	8-Pin CerDIP	–25°C to +85°C
TC430MJA	8-Pin CerDIP	–55°C to +125°C

PIN CONFIGURATION



BONDING DIAGRAM



NOTES:
1. Back of die is common to V_{DD}.
2. Bak if die is not metalized

ABSOLUTE MAXIMUM RATINGS

Power Dissipation at +25°C
- Plastic ..... 1000 mW
- CerDIP ..... 800 mW

Derating Factors
- Plastic ..... 8 mW/°C
- CerDIP ..... 6.4 mW/°C

Supply Voltage ..... $V_{DD} - V_{SS} \leq 15V$
$V_{DD} - V_{DR} \leq 15V$

Input Voltage, Any Terminal ..... V_{DD} +0.3V

Operating Temperature Range
- M Version ..... –55°C to +125°C
- I Version ..... –25°C to +85°C
- C Version ..... 0°C to +70°C

Maximum Chip Temperature ..... 150°C

Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
CerDIP $R_{\theta-JA}$ ..... 150°C/W
Plastic $R_{\theta-JA}$ ..... 125°C/W
ESD Protection 2000V

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

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ELECTRICAL CHARACTERISTICS: T_A = +25°C with $4.5V \leq (V_{DD} - V_{DR}) \leq 12V$, $4.5V \leq (V_{DD} - V_{SS}) \leq 12V$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Logic 1, High Input Voltage		2.4	1.6		V
V_{IL}	Logic 0, Low Input Voltage			1.3	0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	–10		10	µA
V_{OH}	High Output Voltage		V_{DD}–0.025			V
V_{OL}	Low Output Voltage				V_{SS}+0.025	V
R_O	Output Resistance	V_{IN} = 0V, I_{OUT} = 10 mA, V_{SS} = 0V, V_{DD} = 12V		3	5	Ω
		V_{IN} = 3V, I_{OUT} = 10 mA, V_{SS} = 0V, V_{DD} = 12V		3	5	Ω
I_{PK}	Peak Output Current	V_{DD} = 12V		3		A
t_{SKEW1}	Output Pulse Skew	Figure 2		3	5	ns
t_{SKEW2}	Output Pulse Skew	Figure 2		3	5	ns
t_R	Rise Time	Figure 1 C_L = 2200 pF, V_{DD} = 12V		22	30	ns
t_F	Fall Time	Figure 1 C_L = 2200 pF, V_{DD} = 12V		22	30	ns
t_{D1}	Delay Time	Figure 1		18	25	ns
t_{D2}	Delay Time	Figure 1		18	25	ns
I_S	Quiescent Power Supply Current	V_{IN} = 3V, V_{DD} = 12V, V_{SS} = 0V V_{IN} = 0V, V_{DD} = 12V, V_{SS} = 0V		2.9	5 0.3	mA mA

NOTE: Switching times are guaranteed by design.

TC430

ELECTRICAL CHARACTERISTICS: $4.5V \leq (V_{DD} - V_{DR}) \leq 12V$; $4.5V \leq (V_{DD} - V_{SS}) \leq 12V$, $T_A = -55°C$ to $+125°C$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Logic 1, High Input Voltage		2.4			V
V_{IL}	Logic 0, Low Input Voltage				0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	–10		10	µA
V_{OH}	High Output Voltage		V_{DD}–0.025			V
V_{OL}	Low Output Voltage				V_{SS}+0.025	V
R_O	Output Resistance	$V_{IN} = 0V$, $I_{OUT} = 10$ mA, $V_{SS} = 0V$, $V_{DD} = 12V$		4.5	7	Ω
		$V_{IN} = 3V$, $I_{OUT} = 10$ mA, $V_{SS} = 0V$, $V_{DD} = 12V$		4.5	7	Ω
I_{PK}	Peak Output Current	$V_{DD} = 12V$		3		A
t_{SKEW1}	Output Pulse Skew	Figure 2		5	10	ns
t_{SKEW2}	Output Pulse Skew	Figure 2		5	10	ns
t_R	Rise Time	Figure 1 $C_L = 2200$ pF, $V_{DD} = 12V$			40	ns
t_F	Fall Time	Figure 1 $C_L = 2200$ pF, $V_{DD} = 12V$			40	ns
t_{D1}	Delay Time	Figure 1			35	ns
t_{D2}	Delay Time	Figure 1			35	ns
I_S	Quiescent Power Supply Current	$V_{IN} = 3V$, $V_{DD} = 12V$, $V_{SS} = 0V$ $V_{IN} = 0V$, $V_{DD} = 12V$, $V_{SS} = 0V$		5	8 0.5	mA mA

NOTE: Switching times are guaranteed by design.

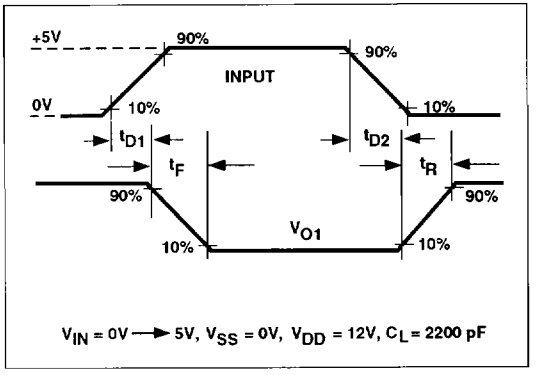


Figure 1 Driver Switching Time

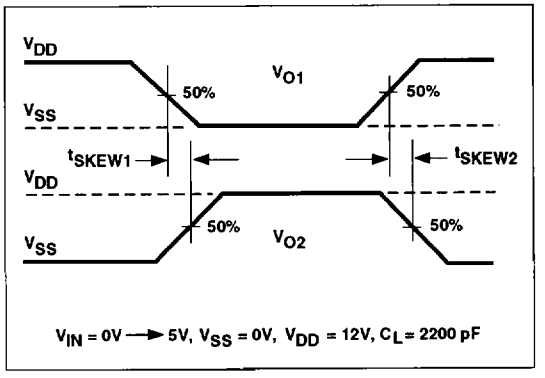
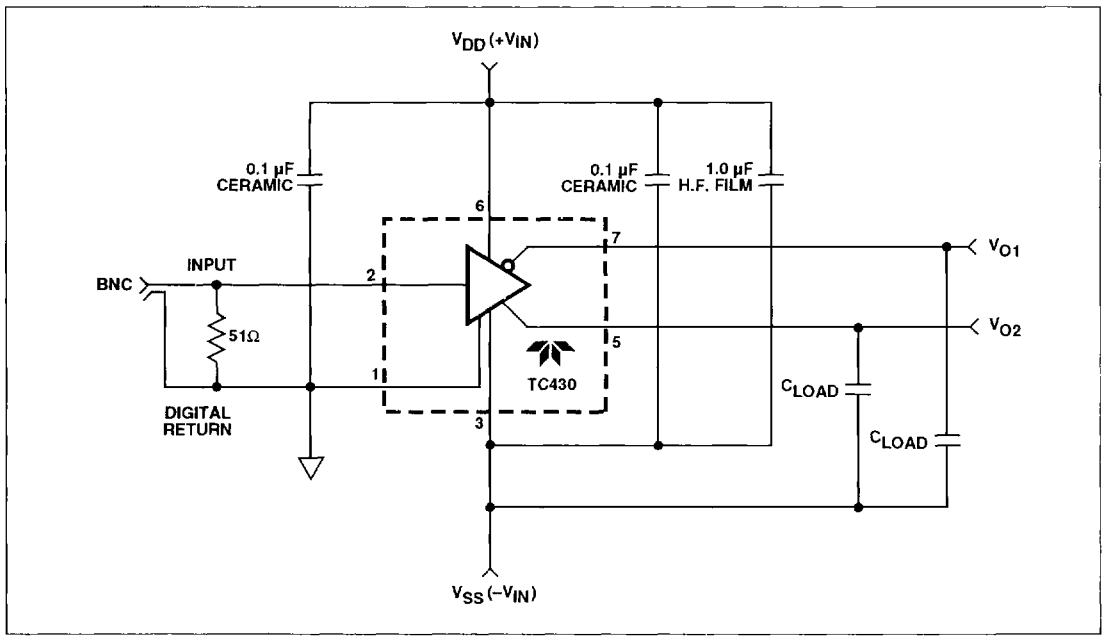


Figure 2 Output Drive Skew

TEST CIRCUIT



APPLICATIONS INFORMATION

Functional Description

The TC430 is fabricated with a super-fast silicon gate process. The input stage consists of a Schmitt trigger which drives a level shift circuit. The level shift circuit allows the input signal to be referenced to some point other than the output return, pin 3 (V_{SS}). This allows the output to swing positive and negative relative to the digital return (pin 1).

The output stage is a low-impedance MOSFET totem pole that can source or sink currents up to 3A peak. This type of output can swing to within millivolts of either rail when driving capacitive loads. Output rise times are on the order of 3 ns, while propagation delays are in the 15 ns region.

Application Tips

Due to its high speed and short transition times, proper layout of the PC board is critical. See Application Note 28 for further information on the effects of layout.

Additional precautions that must be made in addition to those in Application Note 28 are:

(1) Decoupling between the digital return and V_{DD} is critical.

(2) A minimum 4.5V must be maintained between digital return and V_{DD}.

(3) Decoupling between V_{DD} and V_{SS} is critical.

(4) Single-point (star) ground systems should be used.

For decoupling between digital return and V_{DD} [item (1) above] a 1 µF 50V polyester film cap (such as a Wima MKS-2) in parallel with a multilayer ceramic 0.1 µF 50 X7R (such as an AVX dip guard) will work well. These capacitors have to be mounted as close as possible to the respective pins on the TC430 to minimize circuit inductance.

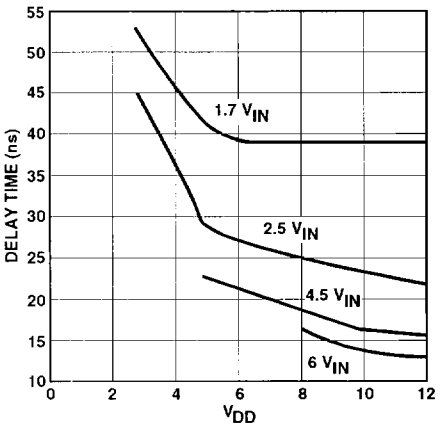
Circuits that are improperly decoupled will exhibit oscillations on the output.

A minimum 4.5V between digital return and V_{DD} [item (2) above] is necessary to ensure that the level shifting and hysteresis circuits have enough voltage to function properly. Put another way, the input circuit is referenced to the positive supply, not the negative supply.

Decoupling of the V_{SS} to V_{DD} [item (3) above] is important because of the high peak current capability of the output of the TC430. The suggested decoupling is a low ESR polyester film capacitor (such as the 1 µF 50V MKS-2) and a ceramic capacitor (such as the AVX 0.1 µF 50V dip guard).

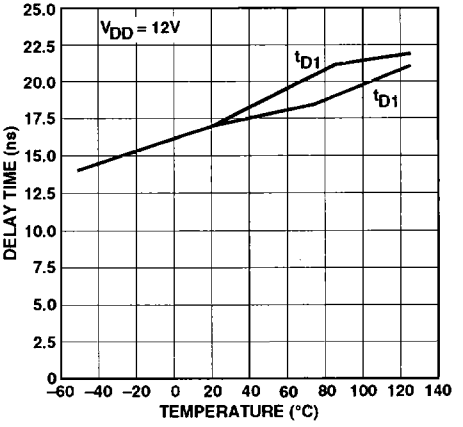
TC430

Delay Time vs V_{DD}



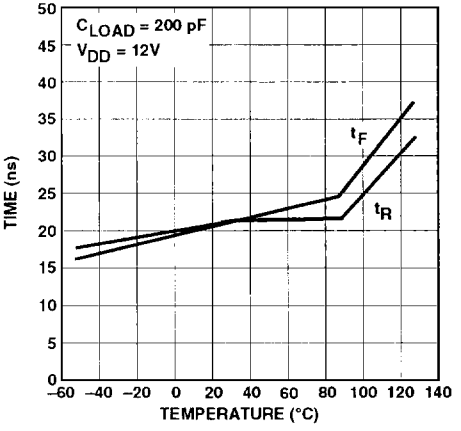
NOTE: Digital return tied to V_{SS}.

Delay Time vs Temperature

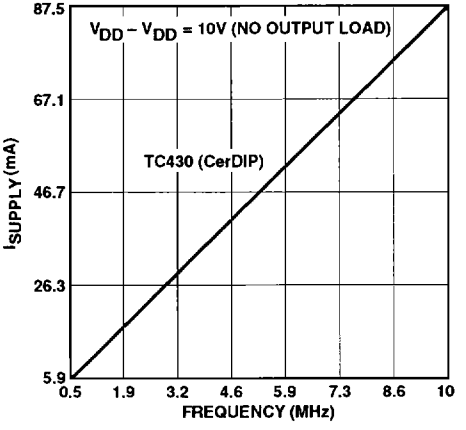


NOTE: Digital return tied to V_{SS}.

Rise/Fall Times vs Temperature



Supply Current vs Frequency



NOTE: Digital return tied to V_{SS}.

The parallel combination of the two capacitors forms a low-impedance source of power across a broad frequency range for the output stage. This will ensure that for any load and frequency of operation the output will be as "clean" as is practical.

The use of single-point grounds [item (4) above] is very critical. Due to the high peak currents that the TC430 is capable of generating, any additional trace or wire length can cause L di/dt drops that can effect the output and in the extreme cause the device to fail due to voltage breakdown.

Application Note 28 explains parasitic inductance problems further.

Operation From a Single Supply

If the TC430 is operated from a single supply voltage, the digital return pin must be tied to the V_{SS} pin. This eliminates the need for the decoupling capacitors from V_{DD} to digital return.

Load Return Path

It is very important to return the load currents directly to, and in the shortest possible distance to V_{SS}, pin 3. Again, this is due to the parasitic inductance of the PC board trace or wire. The test circuit shows how the load capacitors, C_{LOAD}, are returned to the same point as the decoupling capacitors which is directly on pin 3.

Input Signal Considerations

The amplitude of the input signal has a significant effect on the propagation delay through the IC.

While the device can be driven with a signal as small as 2V, propagation delays will be in the 40 ns region. If the input is increased to 5V, delays will be in the 15 ns region.

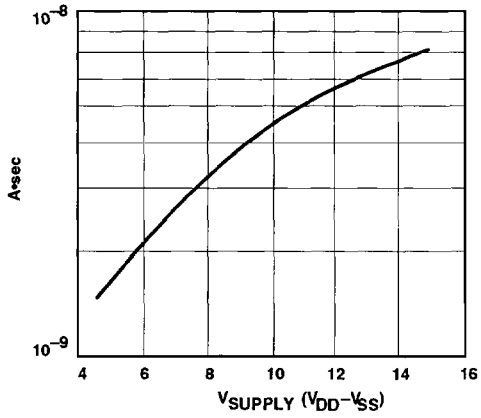
The input stage of the TC430 is a MOSFET gate. Thus, it is of high impedance and requires little drive current. This eliminates the need for speed-up capacitors as with older bipolar parts. The use of speed-up capacitors is not recommended, as they can cause voltage-doubling effects that can be detrimental to the life of the device.

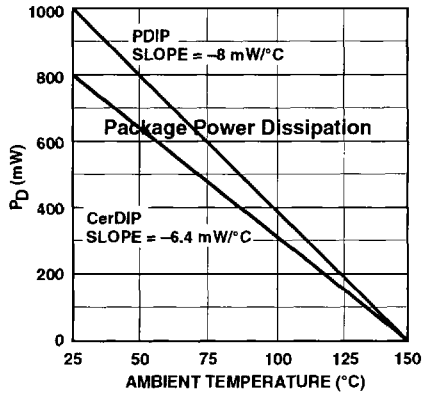
Table I Maximum Operating Frequency

V_S	Max Frequency
12V	4 MHz
10V	9.1 MHz
5V	20 MHz

Conditions: 1. CerDIP Package (θ_{JA} = 150°C/W)
2. T_A = 25°C
3. No load

Crossover Energy Loss





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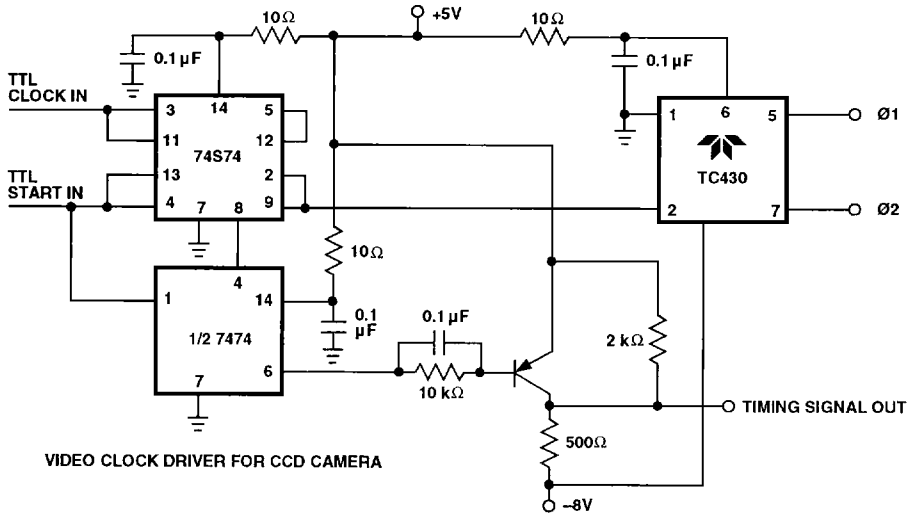
TC430

APPLICATIONS



VIDEO CLOCK DRIVER FOR CCD CAMERA