INDEX

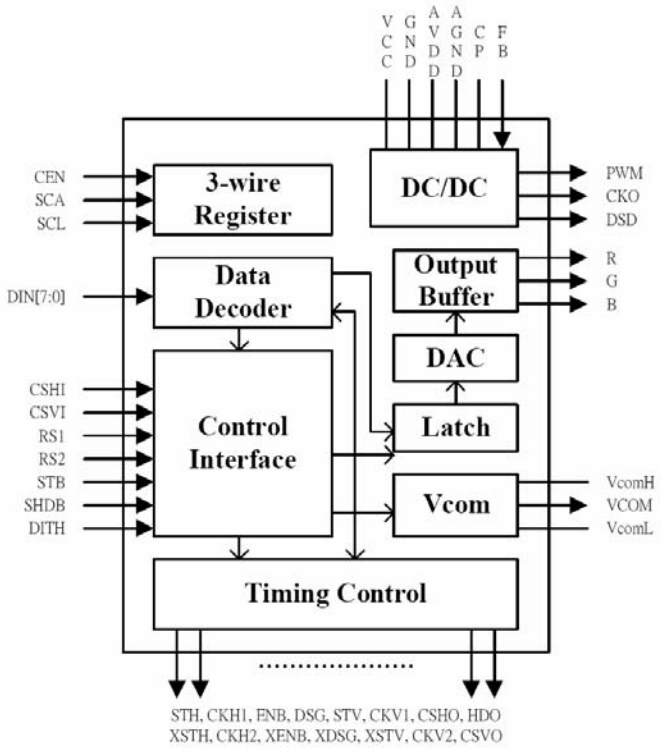
Features

- Handles digital signals of serial 8bit RGB Data
- Installed timing controller to drive LCD panel
- Output: 3 output channels
- Inputs : Digital 8 bit serial data (RGB or YUV– 4:2:2), LCDCLK, synchronous pulse (HD, VD), 3-wire serial control signals
- Outputs : Analog RGB, Common data , Drain Strage data, LCD panel drive signals
- Supply voltage : Digital 2.7V~3.6V, Analog 3.0V~5.5V
- Panel Dimension : 490x240, 521x218, 558x234, 882x228
- TQFP-64 plastic package

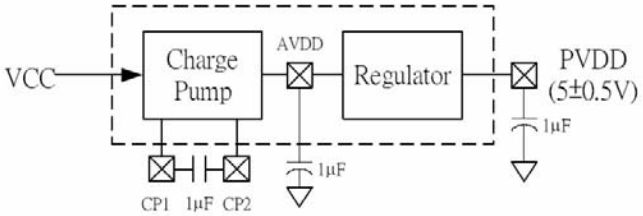
Description

This is digital signal processing IC for low temperature poly-silicon TFT-LCD . Handles 8 bits of input data (256-level gray scale data) for each of the RGB colors and output analog RGB signals from internal OPamp.

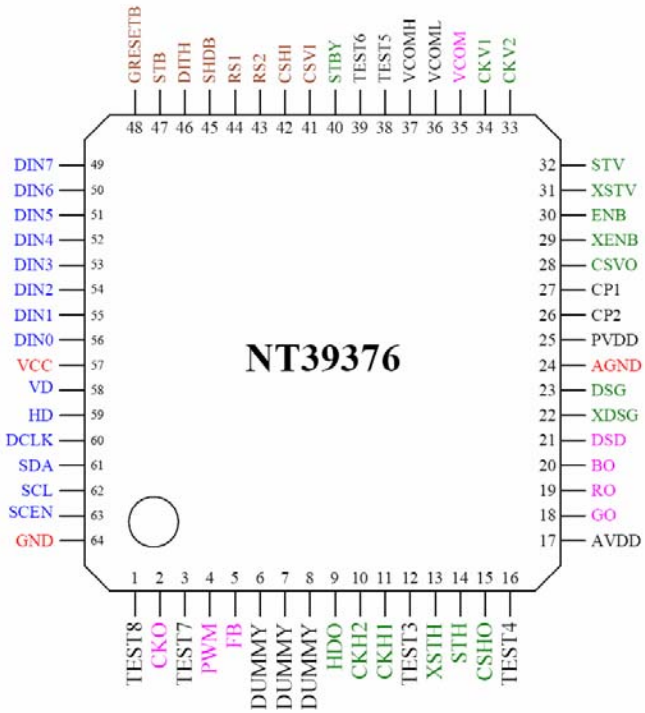
Block Diagram



Charge Pump Circuit



Pin Configuration (IC face view)



Pad Description

Pad No.	Designation	I/O	Description
1	TEST8	T	Testing use
2	CKO	O	Charge pump clock output
3	TEST7	T	Testing use
4	PWM	O	Power transistor gate signal for the boost converter.
5	FB	I	Main boost regulator feedback input. Connect feedback resistive divider to GND. FB threshold is 0.6V nominal.
6	DUMMY	D	Dummy
7	DUMMY	D	Dummy
8	DUMMY	D	Dummy
9	HDO	O	HDO output
10	CKH2	O	H clock pulse 2 output
11	CKH1	O	H clock pulse 1 output
12	Test3	O	Testing use
13	XSTH	O	Inverted STH output
14	STH	O	H start pulse
15	CSHO	O	Switches between Normal scan and Reverse scan (right/left).
16	Test4	O	Testing use
17	AVDD	C	Regulation Capacitor for Analog Voltage. (C_{AVDD} = 1 μF)
18	GO	O	G output
19	RO	O	R output
20	BO	O	B output
21	DSD	O	Pre-charge voltage output
22	XDSG	O	Inverted DSG output
23	DSG	O	Pre-charge pulse output
24	AGND	P	Analog ground
25	PVDD	C	Regulation Capacitor for Charge Pump. (C_{PVDD} = 1 μF)
26	CP2	C	Capacitor for Charge Pump. (C_{cp} = 1 μF)
27	CP1	C	Capacitor for Charge Pump.
28	CSVO	O	Switches between Normal scan and Reverse scan (up/down) .
29	XENB	O	Inverted ENB output
30	ENB	O	Enable pulse output
31	XSTV	O	Inverted STV output
32	STV	O	V start pulse output
33	CKV2	O	V clock pulse 2 output
34	CKV1	O	V clock pulse 1 output
35	VCOM	O	Common output signal
36	VCOML	C	Capacitor for Vcom low. (C_{VCOML} = 2.2 μF)
37	VCOMH	C	Capacitor for Vcom high. (C_{VCOMH} = 2.2 μF)
38	Test5	T	Testing use
39	Test6	T	Testing use
40	STBY	O	STBY output
41	CSVI	I	Vertical inversion control signal input (Normally pulled low) Please refer to page 17
42	CSHI	I	Horizontal inversion control signal input (Normally pulled low) Please refer to page 17.
43, 44	RS2, RS1	I	Resolution selection, normally pulled high.

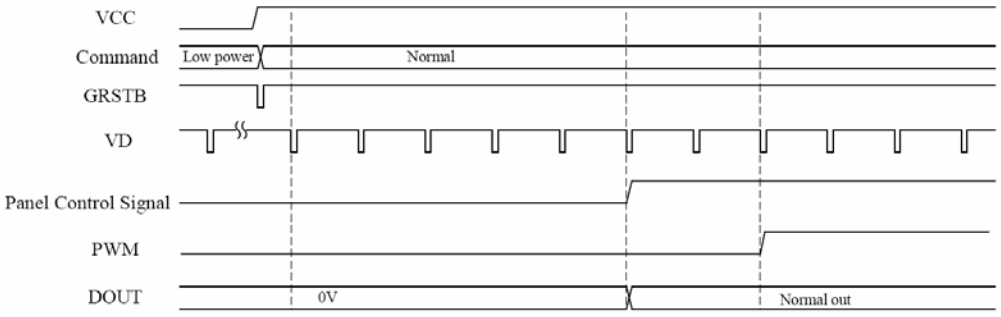
RS1	RS2	Resolution
L	L	490×240
L	H	521×218
H	H	558×234(default mode)
H	L	882×228

45	SHDB	I	Shutdown input. Active low, normally pulled high. (Please refer to page 21.)
46	DITH	I	8-bit dithering. High enable dithering. Low disables dithering and D01, D00 is ignored. Normally pulled low.
47	STB	I	Standby mode setting pin. Active low, Timing Controller, Output Buffer, DAC and DC2DC converter is off when STB is low, normally pulled high.(Please refer to page 21.)
48	GRESETB	I	Global reset pin. It should be connected to VCC in normal operation. If connected to GND, the controller is in reset state, normally pulled high.
49	DIN7	I	Data input. (MSB)
50	DIN6	I	Data input.
51	DIN5	I	Data input.
52	DIN4	I	Data input.
53	DIN3	I	Data input.
54	DIN2	I	Data input.
55	DIN1	I	Data input.
56	DIN0	I	Data input. (LSB)
57	VCC	I	Power supply for digital circuit and charge pump circuit.
58	VD	I	Vertical sync input. Negative polarity.
59	HD	I	Horizontal sync input. Negative polarity
60	DCLK	I	Clock signal; latch data onto line latches at the rising edge.
61	SDA	I/O	Serial Interface data line
62	SCL	I	Serial Interface clock line
63	SCEN	I	Serial Interface chip enable line
64	GND	P	Digital ground

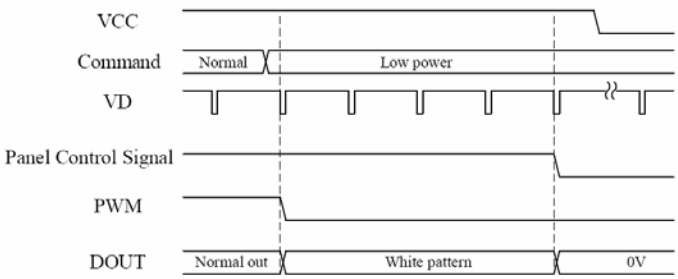
I : Input, **O** : Output, **P** : Power, **C** : Capacitor, **D** : Dummy, **T** : Testing, **I/O** : Input/Output.

Power on/ off and mode change sequence

Power on (low power mode, global reset) to normal mode sequence

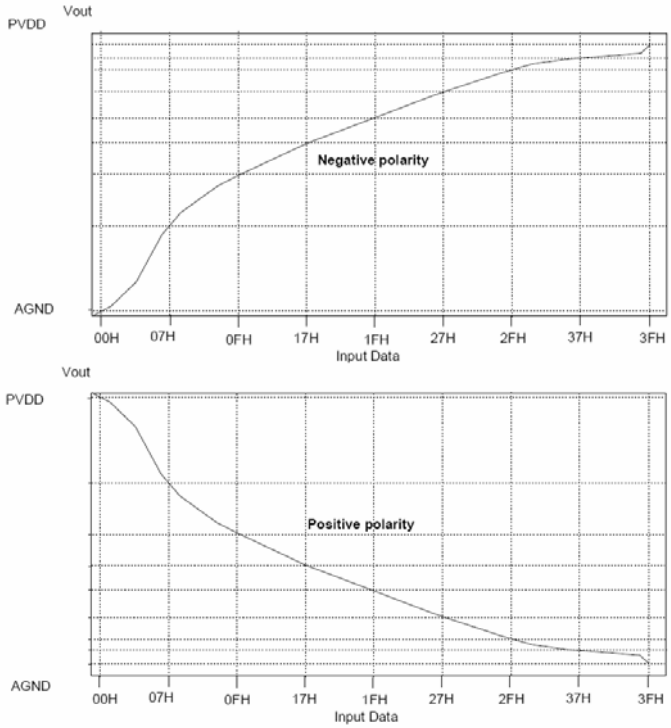


Normal mode to power off (low power mode) sequence



Relationship between input data and output voltage

The figure below shows the relationship between the input data and the output voltage. Please refer to the following pages to get the relative resistor value and voltage calculation method.



Absolute Maximum Ratings*

Logic supply voltage,	V_{CC}	-0.5V to 5V
Storage temperature		-50°C to 100°C
Operating temperature		-30°C to 85°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification are not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{CC} =3.3V, GND=0V, T_A=-30℃~85℃)

For the digital circuit

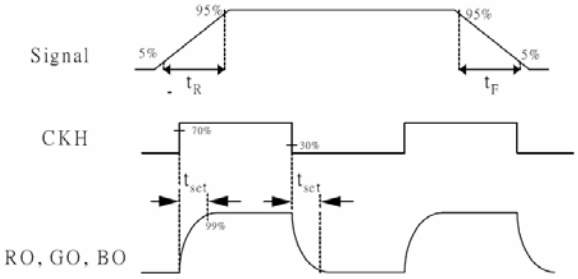
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	2.7	3.3	3.6	V	Digital power
Low Level Input Voltage	V_{il}	GND	-	$0.3\times V_{CC}$	V	Digital input pins
High Level Input Voltage	V_{ih}	$0.7\times V_{CC}$	-	VCC	V	Digital input pins
Input Leakage Current	I_i	-	-	±1	μA	Digital input pins
Pull-high/low Impedance	R_{in}	150k	200k	250k	Ω	
Digital Stand-by Current	I_{st}	-	-	50	μA	DCLK is stopped, Outputs are High-Z Without pull high or low current.
Digital Operating Current	I_{CC}	-	-	13	mA	DCLK=27MHz, V_{CC}=3.3V, PWM no load, RS[2:1]=HL(882×228)

For the analog circuit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Internal Supply Voltage	AV_{DD}	5.0	5.5	6.0	V	Power supply for the analog circuit
	PV_{DD}	4.5	5.0	5.5		Power supply for the gamma resistor
Voltage Deviation of Outputs	V_{vd}	-	±15	±20	mV	V_O =0.5V ~ AVDD-0.5V
Dynamic Range of Output	V_{dr}	0.1	-	AV_{DD}-0.1	V	RO, GO, BO
Low-Level Output Current of Vcom	I_{OLC}	-	20	-	mA	V_{COM} output=0.1V vs. 1.0V(External)
High-Level Output Current of Vcom	I_{OHC}	-	20	-	mA	V_{COM} output=4.9V vs. 4.0V(External)
Low-Level Output Current	I_{OL}	-	-6.0	-	mA	RO, GO, BO; V_O=0.6V v.s. 1.5V(External)
High-Level Output Current	I_{OH}	-	6.0	-	mA	RO, GO, BO; V_O=4.4V v.s. 3.5V(External)
Analog Stand-by Current	I_{st}	-	-	10	μA	STB="0", V_{CC}=3.3V
Analog Operating Current	I_{DD}	-	-	2	mA	V_{CC}=3.3V, Line inversion, RGB no load, Vcom no load, no load, CKO(100kHz) no load
PWM output voltage	V_{PWM}	0	-	V_{CC}	V	
Feed back voltage	V_{FB}	0.55	0.6	0.65	V	DC/DC operating
Base drive current	I_{PWMD}	-	-	1	mA	VPWM output=3.3V vs. 2.6V(External)
Base sink current	I_{PWMS}	-	-	1	mA	VPWM output=0V vs. 0.7V(External)

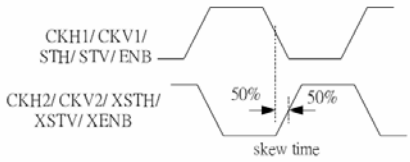
Rise/Fall time

Function pin	Symbol	Min.	Typ.	Max.	Unit	Conditions
CKH1, CKH2, STH, XSTH	t_{HR}	--	--	50	ns	V_{CC}=3.3V Loading condition as Output Loading
	t_{HF}	--	--	50	ns	
CKV1, CKV2, STV, XSTV	t_{VR}	--	--	50	ns	
	t_{VF}	--	--	50	ns	
CSVO, CSHO	t_{CSR}	--	--	50	ns	
	t_{CSF}	--	--	50	ns	
DSG, DSD,	t_{PCR}	--	--	50	ns	
	t_{PCF}	--	--	50	ns	
HDO	t_{HDOR}	--	--	50	ns	
	t_{HDOF}	--	--	50	ns	
RO, GO, BO	t_{set}		65	75	ns	V_{CC}=3.3V, Output high=3.7V, low=0.8V, 1% to 99% (882x228)
			65	75	ns	V_{CC}=3.3V, Output high=3.7V, low=0.8V, 1% to 99% (882x228)
Vcom	t_{VCOM}		TBD	TBD	ns	
			TBD	TBD	ns	

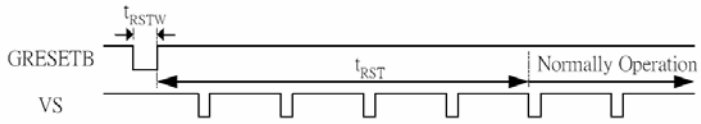


Skew time

Function pin	Symbol	Min.	Typ.	Max.	Unit	Condition
CKH1 vs.CKH2	t_{Skew}	-15	--	15	ns	50% to 50 %
STH vs. XSTH		-15	--	15	ns	50% to 50 %
CKV1 vs. CKV2		-15	--	15	ns	50% to 50 %
STV vs. XSTV		-15	--	15	ns	50% to 50 %
ENB vs. XENB		-15	--	15	ns	50% to 50 %



Global Reset

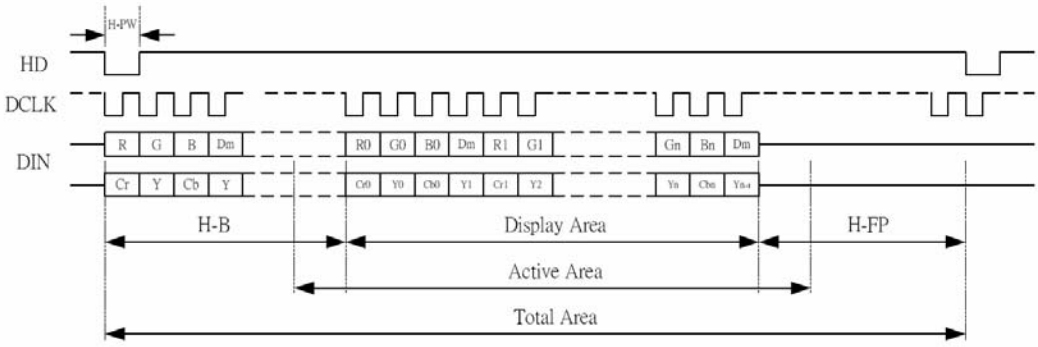


Function pin	Symbol	Min.	Typ.	Max.	Unit	Condition
GRESETB	t_{RSTW}	100	--	--	ns	V_{CC}=3.3V
	t_{RST}	4	--	--	field	

Input timing

1. Serial RGBdummy or YUV-4:2:2 Mode (This mode is only for 558×234 and 882×228)

Horizontal



Input Format	Format Standard	DCLK(MHz)	H-PW$_{min}$	Total AREA	Active AREA	Display AREA	H-B	H-FP
YUV	ITUR601-NTSC	f_{DCLK} = 27	1	1716	1440	1328 (1400)	296 (260)	92(56)
	ITUR601-PAL			1728				104(68)
RGBdummy	QVGA	f_{DCLK} = 25	1	1560	1280	1228 (1216)	268 (272)	64 (72)
	NTSC	f_{DCLK} = 24.54						
	PAL	f_{DCLK} = 24.38						

(unit : DCLK)

( ) : for 558*234

YCbCr to RGB conversion

Format A

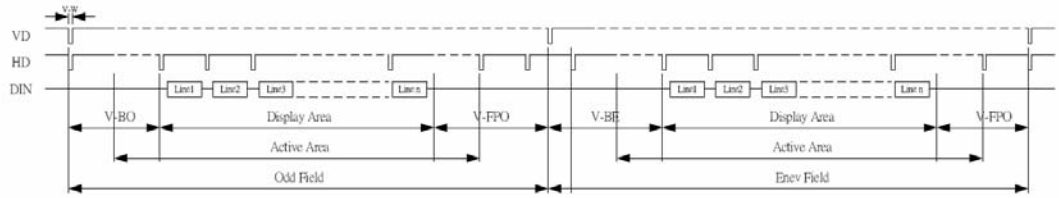
$$\begin{cases} R=Y+1.402Cr \\ G=Y-0.714Cr-0.344Cb; \ [Y=0\sim255, Cr \ \&Cb=-128\sim127] \\ B=Y+1.772Cb \end{cases}$$

Format B

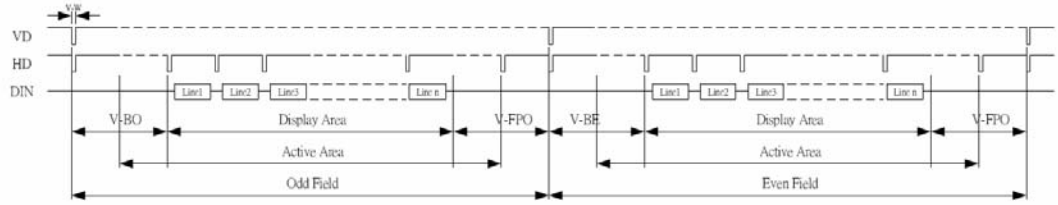
$$\begin{cases} R=1.16(Y-16)+1.60(Cr-128) \\ G=1.16(Y-16)-0.81(Cr-128)-0.39(Cb-128); \ [Y=16\sim235, Cr \ \&Cb=16\sim240] \\ B=1.16(Y-16)+2.02(Cb-128) \end{cases}$$

Vertical

Interlace



Non-interlace

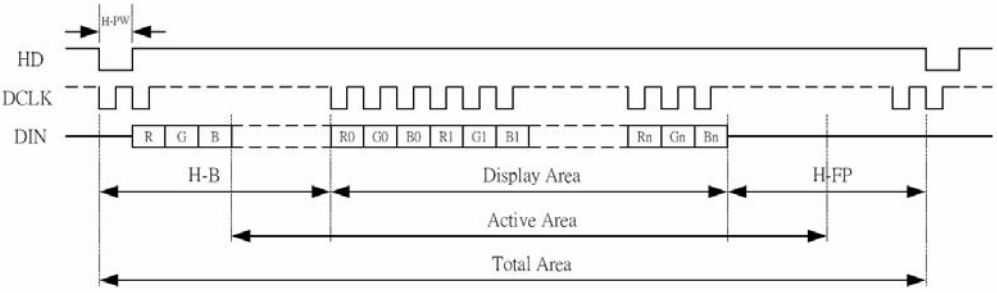


Mode		Interlace						None interlace		
		Odd			Even					
Format Standard		QVGA	NTSC / ITUR601	PAL / ITUR601	QVGA	NTSC / ITUR601	PAL / ITUR601	QVGA	NTSC / ITUR601	PAL / ITUR601
Scaling down display area	490×240	240			240			240		
	521×218	218			218			218		
	558×234	234			234			234		
	882×228	228			228			228		
Active area		240		288	240		288	240		288
Total area		262.5		312.5	262.5		312.5	262		312
V-B	490×240	21		24	21.5		24.5	21		24
	521×218	32		24	32.5		24.5	32		24
	558×234	24		24	24.5		24.5	24		24
	882×228	27		24	27.5		24.5	27		24
V-FP	490×240	1.5		0.5	1		0	1		0
	521×218	12.5		0.5	12		0	12		0
	558×234	4.5		0.5	4		0	4		0
	882×228	7.5		0.5	7		0	7		0

(unit : H)

2. Through Mode

Horizontal



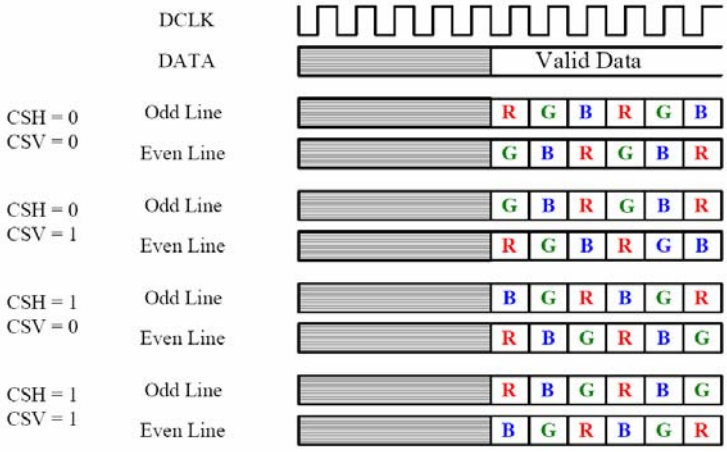
Panel dot	DCLK	SR Qty	H-PW$_{min}$	Total AREA	Active AREA	Display AREA	H-B	H-FP
490*240	T_{DCLK} = 102.2nS	164	1	622	539	492	103	27
521*218	T_{DCLK} = 90.54nS	175	1	702	573	525	130	47
558*234	T_{DCLK} = 90.54nS	187	1	702	614	561	130	11
882*228	T_{DCLK} = 55.46nS	295	1	1146	969	885	190	71

(unit : DCLK)

H-W condition : 3n+1

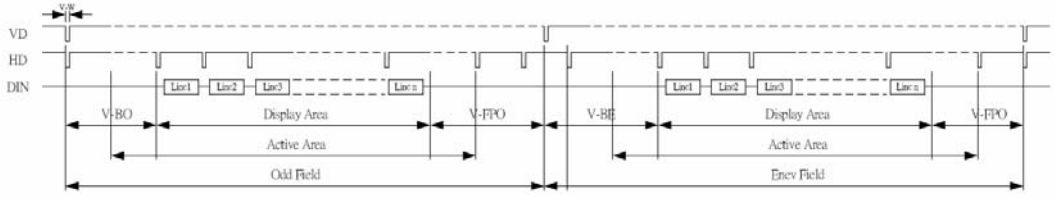
Input RGB Sequence

490x240,521x218,558x234,882x228

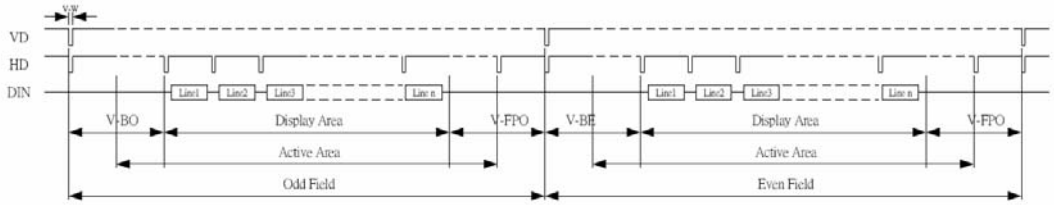


Vertical

Interlace



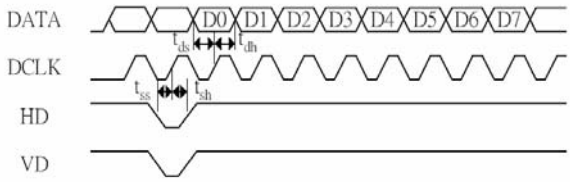
Non-nterlace



Mode	Interlace								None interlace			
	Odd				Even							
(Scaling down)Display area	240	218	234	228	240	218	234	228	240	218	234	228
Active area	240				240				240			
Total area	262.5				262.5				262			
V-B	21	32	24	27	21.5	32.5	24.5	27.5	21	32	24	27
V-FP	1.5	12.5	4.5	7.5	1	12	4	7	1	12	4	7

(unit : H)

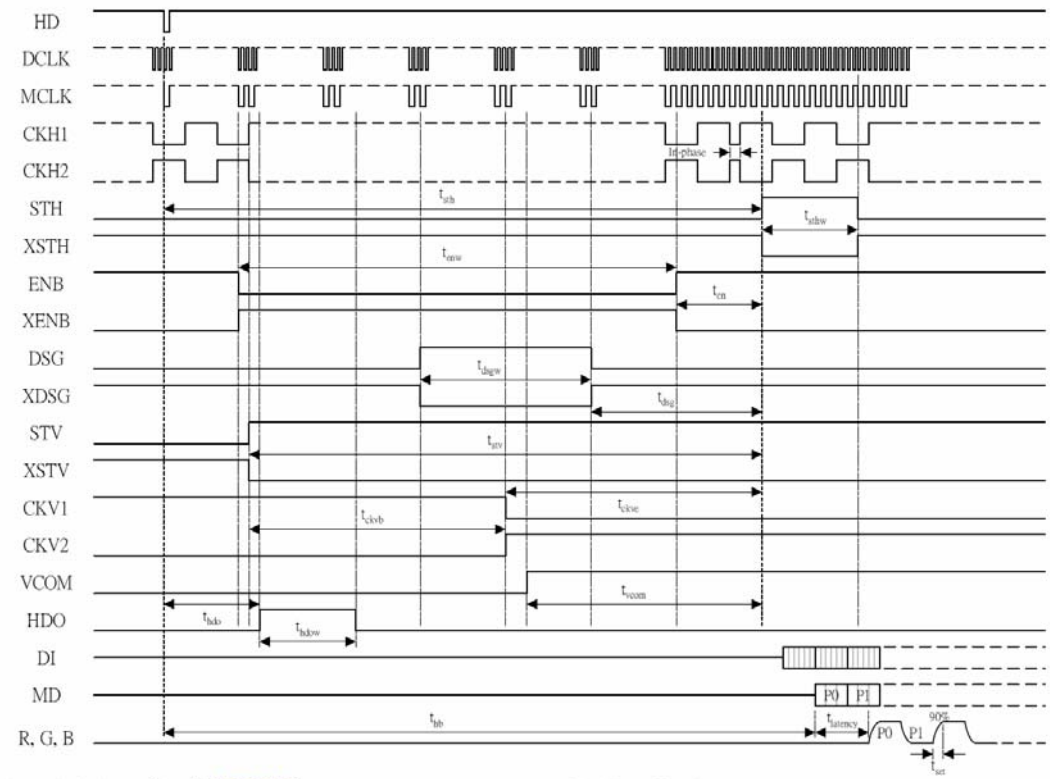
Timing Diagram



Item	Symbol	Min	Typ	Max	Unit
DCLK duty ratio	Duty	40	--	60	%
Data setup time	T_{dsu}	12	--	--	ns
Data hold time	T_{dhd}	12	--	--	ns
Sync. signal setup time	T_{csu}	12	--	--	ns
Sync. signal hold time	T_{chd}	12	--	--	ns

Output Timing

Serial RGBdummy or YUV-4:2:2 Horizontal Mode Output Timing



$t_{sth} = t_{hb} + t_{latency} - (t_{sthw} + 1LCDCLK)$

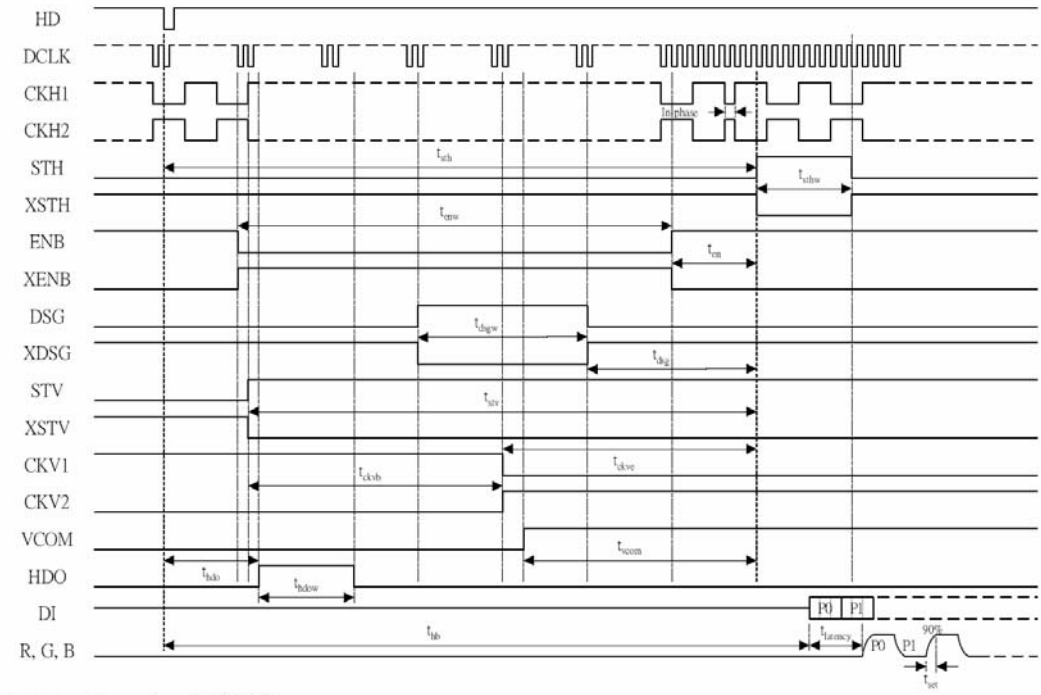
Symbol	Panel Resolution				Unit	Condition
	558*234		882*228			
Format	YUV	RDBDm	YUV	RDBDm		
t_{hb}	260	272	296	268	DCLK	V_{CC}=3.3V
$t_{latency}$	39	23.5	33.5	19	DCLK	
t_{sth}(*)	264	265	308.5	267.5	DCLK	
t_{sthw}(*)	13	13	13	13	LCDCLK	
t_{en}(*)	15	14	32	32	LCDCLK	
t_{enw}(*)	82	77	125	125	LCDCLK	
t_{dsg}(*)	26	24	40	40	LCDCLK	
t_{dsgw}(*)	30	28	63	63	LCDCLK	
t_{stv}(*)	94	88	148	148	LCDCLK	
t_{ckve}	41	38	95	95	LCDCLK	
t_{ckvb}	53	50	53	53	LCDCLK	
t_{vcom}	40	37	122	122	LCDCLK	
t_{hdo}(*)	22	22	22	22	LCDCLK	
t_{hdow}(*)	32	32	32	32	LCDCLK	

(*) is programmable by 3-wire register

Scaling Ratio

Resolution	558*234		882*228	
Input Format	YUV	RGBDm	YUV	RGBDm
Active area	1440	1280	1440	1280
Display area	1400	1216	1328	1228
Display/4	350	304	332	307
Scale ratio	1.871	1.626	1.125	1.04
Display dots	561	561	885	885

Through Mode Output Timing



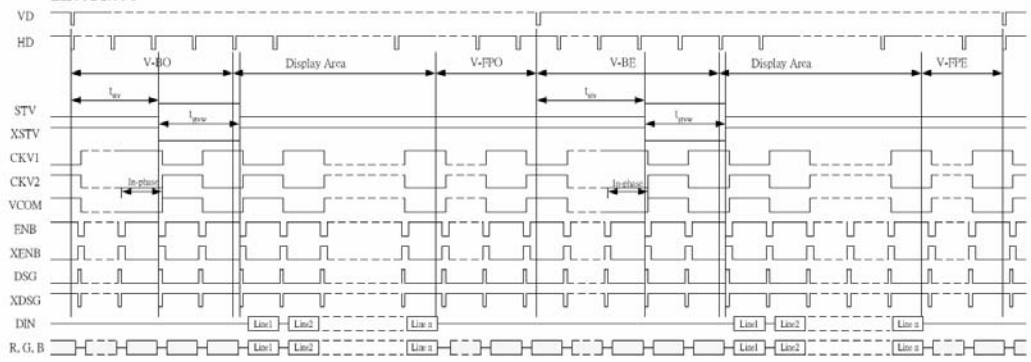
t_{sth} = t_{hb} + $t_{latency}$-(t_{sthw}+1DCLK)

Symbol	Panel Resolution				Unit	Condition
	490*240	521*218	558*234	882*228		
t_{hb}	103	130	130	190	DCLK	V_{CC}=3.3V
$t_{latency}$	6.5	6.5	6.5	6.5	DCLK	
t_{sth}(*)	95.5	122.5	122.5	182.5	DCLK	
t_{sthw}(*)	13	13	13	13	DCLK	
t_{en}(*)	12	15	15	32	DCLK	
t_{enw}(*)	69	80	80	125	DCLK	
t_{dsg}(*)	22	22	25	40	DCLK	
t_{dsgw}(*)	25	29	29	63	DCLK	
t_{stv}(*)	79	92	92	148	DCLK	
t_{ckve}	35	40	40	95	DCLK	
t_{ckvb}	44	52	52	53	DCLK	
t_{vcom}	30	39	39	122	DCLK	
t_{hdo}(*)	22	22	22	22	DCLK	
t_{hdow}(*)	32	32	32	32	DCLK	

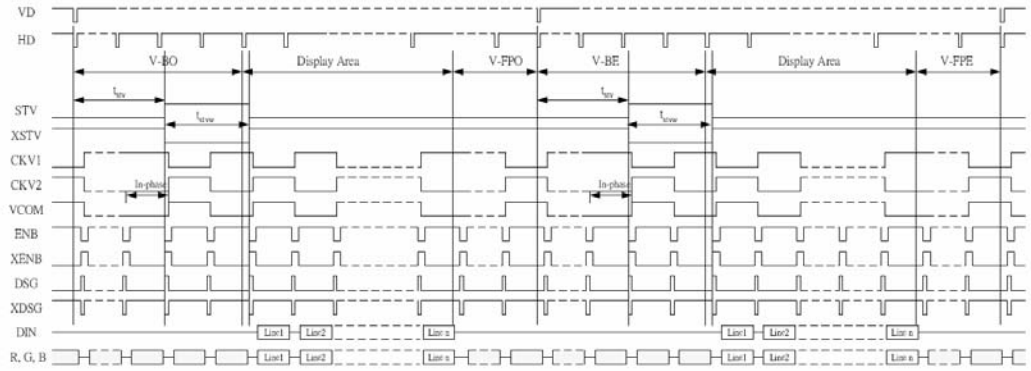
(*) is programmable by 3-wire register

Vertical

Interlace



Non-Interlace

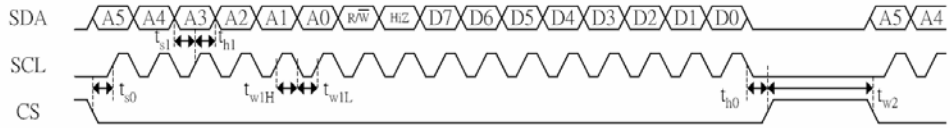


Mode	Interlace								None interlace			
	Odd				Even							
Display area	240	218	234	228	240	218	234	228	240	218	234	228
V-B	21	32	24	27	21.5	32.5	24.5	27.5	21	32	24	27
t_{stv}	19	30	22	25	19.5	30.5	22.5	25.5	21	32	24	27
t_{stvw}	2	2	2	2	2	2	2	2	2	2	2	2

(unit : H)

3-Wires Serial Control Interface

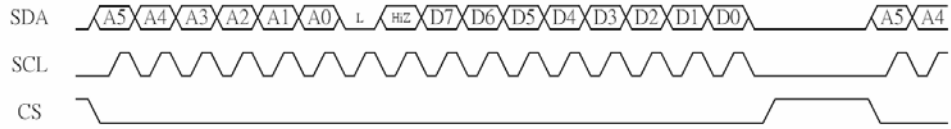
3 wires Serial data transfer format



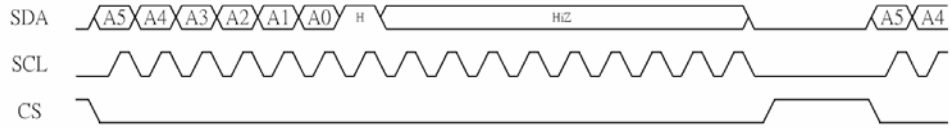
Item	Symbol	Conditions	Min	Typ	Max	Unit
SDA Setup Time	t_{s0}	SCEN to SCL	150			ns
	t_{s1}	SDA to SCL	150			ns
SDA Hold Time	t_{h0}	SCEN to SCL	150			ns
	t_{h1}	SDA to SCL	150			ns
Pulse Width	t_{w1L}	SCL pulse width	160			ns
	t_{w1H}	SCL pulse width	160			ns
	t_{w2}	SCEN pulse width	1.0			us
Clock duty			40		60	%

Note:
1. Only when SCL is input in 16-bit clock while SCEN is in the "Low" period, SDA is accepted at rise of SCEN.
2. If SCL is in 15-bit or 17-bit clock while SCEN is in the "Low" period, SDA is not accepted.
*) It is necessary DCLK input for SDA setting
3. Items are set at fall of the vertical sync.

Write Command



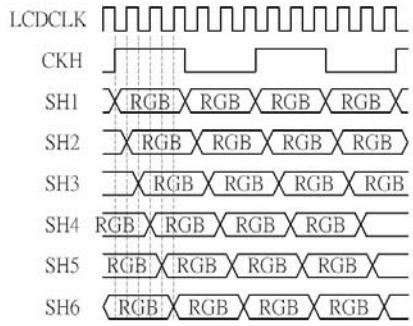
Read Command



Register description

Address	Register Name	Read/Write	Default	Meaning	Note
0x01	Chip ID	R	0x31	[7:4]: Chip ID [3:0]: Chip version	
0x02	Input select	R/W	0xCD	[1:0]: Input format 00: Serial RGBDummy 01: Serial YUV 10: Through mode [4:2]: Format Standard 000: QVGA(25MHz) 001: NTSC(24.54MHz) 010: PAL(24.38MHz) 011: ITUR-601-NTSC(27MHz) 100: ITUR-601-PAL(27MHz) 101~111: invalid [5]: Input clock latch data edge 0: positive edge 1: negative edge [6]: HD polarity 0: positive polarity 1: negative polarity [7]: VD polarity 0: positive polarity 1: negative polarity	
0x03	Sample/Hold phase	R/W	0x00	[2:0]: SH Phase 0 0 0: SH1 0 0 1: SH2 0 1 0: SH3 0 1 1: SH4 1 0 0: SH5 1 0 1: SH6 110~111: invalid.	NOTE<0>
0x04	Mode select<1>	R/W	0x10	[1:0]: Input data sampling delay phase for YCrCb mode 00: normal 01: 1 LCDCLK delay 10: 2 LCDCLK delay 11: 3 LCDCLK delay [3:2]: YCrCb sequence for YCrCb mode 00: CrYCbY 01: YCrYCb 10: CbYCrY 11: YcbYCr [4]: YUV input format 0: Format A 1: Format B [5]: UV offset for Format A 0: Straight 1: Offset	NOTE<1>
0x05	Mode select<2>	R/W	0x06	[0]: Select of interlace mode 0: Interlace 1: Non-interlace [1]: Select of field mix 0: Odd-line←Even-Line 1: Even-line←Odd-Line [2]: Pixel Arrangement 0: BRG 1: RGB	NOTE<2>
0x06	Low-power mode select	R/W	0x0D	[1:0]: Low-power mode 00: Standby-mode 01: Normal-mode 10: Sleep-mode 11: Invalid [2]: PWM output 0: PWM off 1: Normally output [3]: CKO output 0: CKO off 1: Normally output	NOTE<3>
0x07	STBY output	R/W	0x00	[0]: STBY output 0: STBY output = Low 1: STBY output = Hi	
0x08	Horizontal Start Position	R/W	0x08	[3:0]: Adjustment 16 step of horizontal phase (unit: 1/2 CKH)	NOTE<4>
0x09	Vertical Start Position	R/W	0x08	[3:0]: Adjustment 16 step of vertical phase (unit: 1H)	NOTE<5>

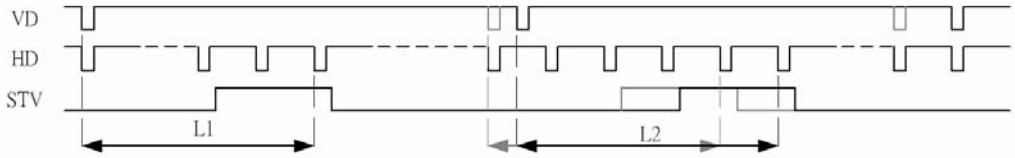
NOTE<0> Sample/Hold phase



NOTE<1> UV offset for Format A

R4[5]	UV range	Note
0	-128~127	U' = U, V' = V
1	0~255	U' = U-128, V' = V-128

NOTE<2> Field mix mode & Interlace mode



L1=t_{vbo}, L2=t_{vbe}. (Refer to page16)

		Interlace		Non-interlace
		R5[0]=0		
		NTSC	PAL	R5[0]=1
Odd line ← Even line	R5[1]=0	L2=L1-0.5	L2=L1+0.5	L2=L1
Even line ← Odd line	R5[1]=1	L2=L1+0.5	L2=L1+1.5	L2=L1

(unit: Horizontal Line)

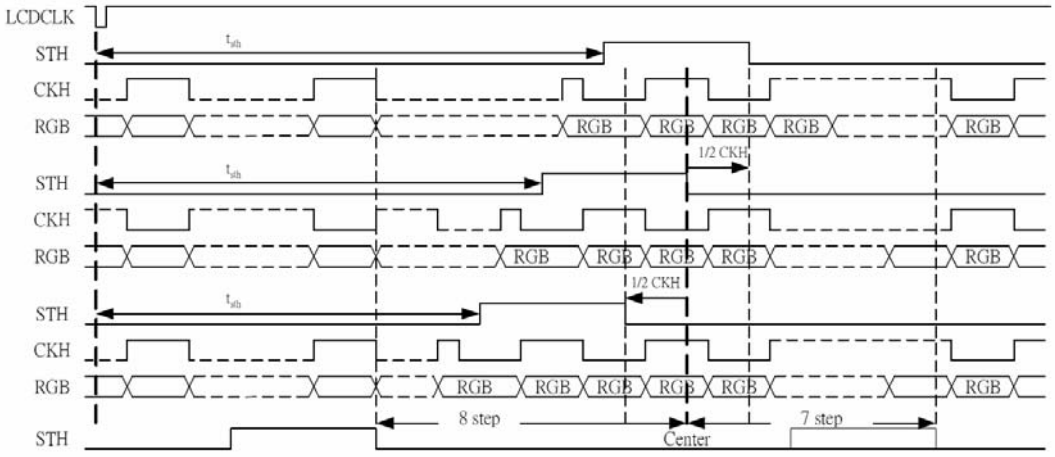
NOTE<3> Power save mode

Input		Register	Output mode
STB	SHDB	R6[1:0]	
High	High	00	Standby
		01	Normal
		10	Sleep
Low	High	00	Standby
		01	
		10	
x	Low	00	Sleep
		01	
		10	

*) Default setting: STB/SHDB pull high.

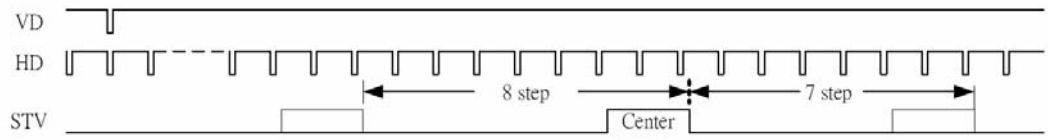
Function pin	Normal	Standby	Sleep
RGB DSD COM	Normal output	Low	Low
CKH1 CKH2	Normal output	CKH1=H CKH2=L	Low
STH XSTH		STH=H XSTH=L	
DSG XDSG		DSG=H XDSG=L	
ENB XENB		ENB=H XENB=L	
CKV1 CKV2		CKV1=H CKV2=L	
STV XSTV		STV=H XSTV=L	
CKO		Low	
PWM		Low	

NOTE<4> Adjustment of horizontal phase (unit : 1/2 CKH)



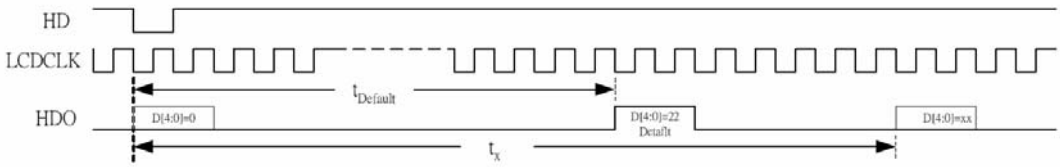
*) While adjusting horizontal phase, STH and CKH must be adjusted simultaneously with relationship between STH and CKH remains the same. And then t_{sth} will charge.

NOTE<5> Adjustment of vertical phase (unit : 1H)



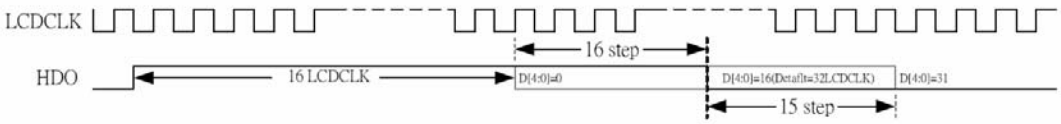
*) STV default timing is refer to page 16.

NOTE<6> Adjustment 64 step of horizontal synchronous pulse phase (unit : 1LCDCLK)



Panel dot	T_{LCDCLK} (nSec)	$t_{Default}$ = 22LCDCLK (µSec)	t_{2uSec} (LCDCLK)
490*240	102.2	2.248	20
521*218	90.54nS	1.992	22
558*234	90.54nS	1.992	22
882*228	55.46nS	1.22	36

NOTE<7> Adjustment 32 Step of horizontal synchronous pulse width (unit : 1LCDCLK)



Panel dot	T_{LCDCLK} (nSec)	$t_{Default}$ = 32LCDCLK (μSec)
490*240	102.2	3.27
521*218	90.54	2.897
558*234	90.54	2.897
882*228	55.46	1.775

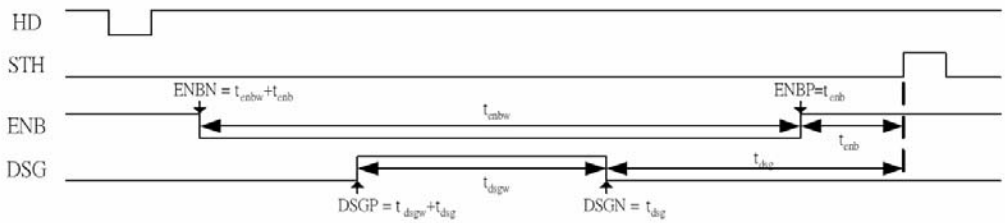
NOTE<8> Reverse mode selection

Input		Output
CSHI	R0C[0]	CSHO
Low	0	Low
	1	High
High	0	High
	1	High

Input		Output
CSVI	R0C[1]	CSVO
Low	0	Low
	1	High
High	0	High
	1	High

*) Default setting: CSHI/CSVI pull Low

NOTE<9> Adjustment of output timing (ENB, DSG, STH) (unit: 1LCDCLK)



*) The default timing of "ENB", "DSG" is refer to page 15.
*) ENBN, ENBP, DSGP, DSGN couldn't be in front of HD falling edge.
(ENBN < ENBP < t_{sth} , DSGP < DSGN < t_{sth})
*) Register Value Setting Rule
$Reg[Addr]_{Value} = Reg[Addr]_{Default} + Reg[Addr]_{Setting} - Reg[Addr]_{Table}$
$Reg[Addr]_{Table}$ are decide by panel resolution and be chose by pin RS1, RS2 (Reference to Output Timing)

Example: The panel resolution is 490*240 , $Reg[0x0E]_{Table}$ = 9, $Reg[0x0E]_{Default}$ = 0x80 and If it want to set ENBB = 10, then The $Reg[0x0E]_{Value}$ must be set as

$$Reg[0x0E]_{Value} = 0x80+0x0A-0x09 = 0x81$$

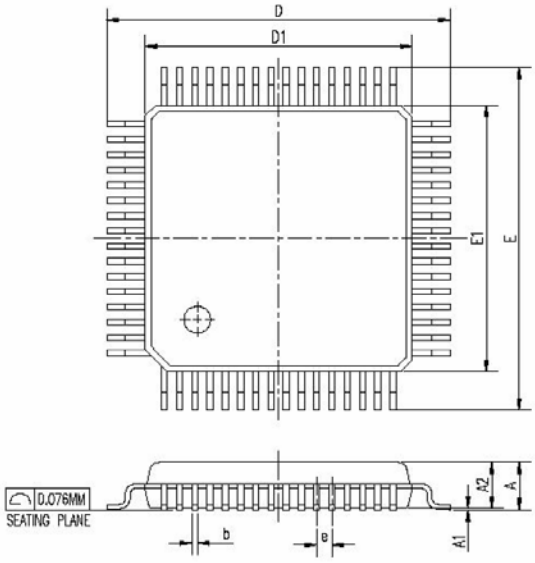
NOTE<10> Adjustment of common

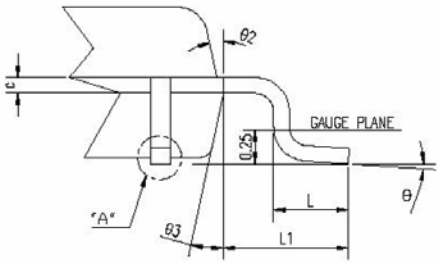
R16	COMH level	Typical Value
00h	PV_{DD}-1.36V	3.64V
28h(default)	PV_{DD} -0.56V	4.44V
3Fh	PV_{DD} -0.1V	4.9V

R17	COML level	Typical Value
00h	AGND+0.1	0.1V
1Bh(default)	AGND+0.64	0.64V
3Fh	AGND+1.36	1.36V

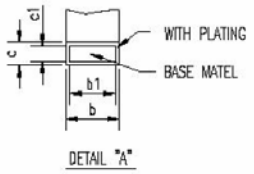
R18	DSD level	Typical Value
00h	PV_{DD} ×0.58+0.64V	3.54V
15h(default)	PV_{DD} ×0.58	3.1V
3Fh	PV_{DD} ×0.58-0.62V	2.28V

Package Dimension (TBD)





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.156			0.046
A1	0.05		0.15	0.002		0.006
A2	0.94	1.00	1.06	0.037	0.039	0.042
c	0.119		0.185	0.005		0.007
c1	0.127 TYP.			0.005 TYP.		
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.95	7.00	7.05	0.273	0.276	0.278
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.95	7.00	7.05	0.273	0.276	0.278
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	1.5	3.5	5.5	1.5	3.5	5.5
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13



	MIN.	NOM.	MAX.	NOM.	MIN.	MAX.	NOM.	MIN.	MAX.
b	0.34		0.45	0.15		0.26	0.15		0.26
b1	0.34	0.37	0.40	0.15	0.18	0.21	0.15	0.18	0.21
e	0.80BSC.			0.50BSC.			0.40BSC.		
N	32			48			64		
JEDEC	MS-026 ABA			MS-026 ABC			MS-026 ABD		