SL811S/T USB Dual Speed Slave Controller Data Sheet

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TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

LIST OF FIGURES

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1.0 Conventions

1,2,3,4	Numbers without annotations are decimals
Dh, 1Fh, 39h	Hexadecimal numbers are followed by an “h”
0101b, 010101b	Binary numbers are followed by a “b”
bRequest, n	Words in italics indicate terms defined by USB Specification or by this specification

2.0 Definitions

USB	**U**niversal **S**erial **B**us
SL811S/T	SL811S/T is a Cypress USB Controller, providing multiple functions on a single chip. The SL811S/T is available in both a 28-pin PLCC package, and a 48-pin LPQFP package (SL811ST)
SL811S/T	SL811S/T refers to both the SL811S and SL811ST. **Note:** This chip does not include a CPU.

3.0 References

[Ref 1] USB Specification 1.1: http://www.usb.org

4.0 Introduction

4.1 Overview

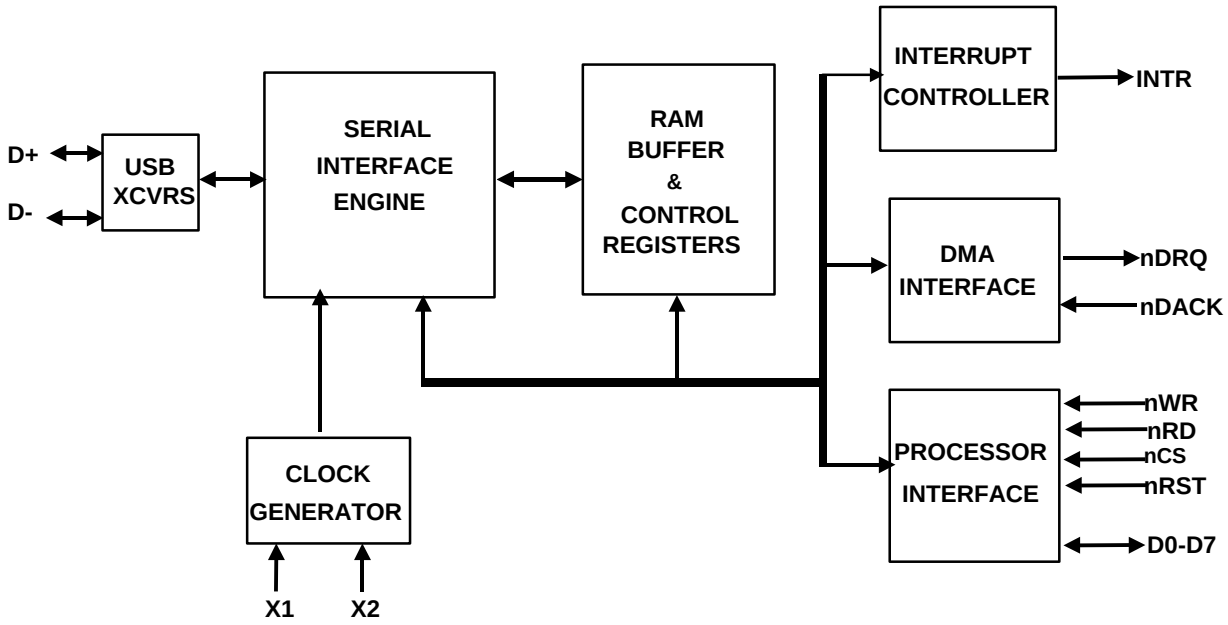
The SL811S/T USB Slave Controller is a single chip USB peripheral device that interfaces to microprocessors. The SL811S/T USB Controller incorporates USB Serial Interface functionality along with internal drivers and receivers that connect directly to the USB interface connector. The SL811S/T supports and operates in USB full speed mode, at 12 Mbits per second and in USB Slow speed mode at 1.5 Mbits per second.

The local host interface provides an 8-bit data path, with interrupt and **DMA** support to allow an easy interface to standard microprocessors or microcontrollers. Internally, the SL811S/T contains a 256-byte RAM data buffer. The RAM contains both control registers and data buffers. SL811S/T comes in two packages - 28-pin PLCC (SL811S) and 48-pin LPQFP (SL811T). Both products require a 3.3 VDC power supply.

The SL811S/T can interface to any microprocessor, microcontroller, or DSP. It can also interface directly to a variety of buses including ISA, PCMCIA and others through its 8-bit bidirectional Data port and through the following control signals - CS, WR, RD, INTR, and A0. Both INTEL and MOTOROLA buses, and others like them, are supported.

The SL811S/T USB Slave Controller is designed to conform to USB specification 1.1 for full-speed, and low speed operation. The USB specification should be referred to as a reference when designing with the SL811S/T.

4.2 Block Diagram



4.3 Features

4.3.1 USB Specification Compliance

- Conforms to USB Specification 1.1

4.3.2 CPU Interface

- Standard Microprocessor Interface
- Supports DMA Transfers
- 256 x 8 SRAM “On-Chip” memory
- 8-bit Bidirectional Data Port, interfaces to any external Bus or CPU (Intel, Motorola, etc.)
- Four USB Endpoints
- On-Chip USB transceivers
- On-Chip full/slow speed USB transceivers
- Supports power suspend mode
- 3.3V power source, CMOS Technology
- Logic interface is 5 Volt tolerant
- Memory buffer includes Double buffer Ping Pong operation scheme
- Operates on either 12-MHz or 48-MHz crystal/clock.
- Auto Address increment mode to simplify memory access and improve performance
- Available in 28-Pin PLCC or 48 LPQFP packages
- Generic WDM Mini Port driver for Windows 98, 2000/NT 5.0, and CE3.0, firmware and system USB demo source examples are available.

4.4 Data Port, Interface to external Micro-Processor

The SL811S/T Data Port interface provides an 8-bit bidirectional data path with appropriate control signals such as CS, RD, WR, A0 and INTR lines. This feature enables it to interface to any external processor or controller (Intel, Motorola, TI, Analog Devices, etc.). The control Read and Write signals, Chip Select and a single address line A0, with the 8-bit data bus, support both programmed I/O or Memory mapped I/O designs.

Access to the memory and control register space is a simple two step process, requiring an address write with A0 set to '0' followed by a register/memory read or write cycle with address line A0 set to '1'.

The SL811S/T write or read operation terminates when either nWR or nCS becomes inactive. For devices interfacing to the SL811S/T that deactivate the Chip Select nCS before the write nWR, the data hold timing should be measured from the nCS and will be the same value as specified. Thus, both Intel and Motorola type CPUs work well with SL811S/T without any external glue logic required.

4.5 DMA Controller

In applications that require transfers of large amounts of data such as scanner interfaces, the SL811S/T provides a DMA interface. This interface supports DMA read or write transfers to the SL811S/T internal RAM buffer through the microprocessor data bus via two control lines: nDRQ (Data Request) and nDACK (Data Acknowledge), and along with the nWR line, controls the data flow into the SL811S/T. The SL811S/T has a count register that allows programmable block sizes to be selected for DMA transfer. The control signals interface—both nDRQ and nDACK—are designed to be compatible with standard DMA interfaces.

4.6 Interrupt Controller

The SL811S/T interrupt controller provides a single output signal. The INTR can be activated by a number of events that may occur as a result of USB activity. Control and status registers are provided to allow you to select single or multiple events that will generate an interrupt (assert INTR), and provide a means of viewing the interrupt status. The interrupt can be cleared by writing to the Status Register located in the internal register space at address 0x0d.

4.7 Buffer Memory

The SL811S/T contains 256 bytes of internal buffer memory. The first 64 bytes of memory represent the control register, status registers, and Endpoint registers for programmed I/O operations. The remaining memory locations are used for data buffering (max 192 Bytes).

Access to the registers and data memory is done by an external microprocessor through the 8-bit data bus. This can be in either of two addressing modes - indexed or direct access. With indexed addressing, the address is first written into the device with the A0 address line Low, then the following cycle with A0 address line High is directed to the specified address. USB transactions are automatically routed to the memory buffer. Control registers are provided to set up pointers and block sizes in buffer memory.

4.8 USB Transceiver

The SL811S/T has a built in transceiver that meets USB Specification 1.1. The transceiver is capable of transmitting and receiving serial data at USB full speed (12 Mbits/sec) and slow speed (1.5 Mbits/sec). The driver portion of the transceiver is differential, while the receiver section is comprised of a differential receiver and two single ended receivers. Internally, the transceiver interfaces to the Serial Interface Engine, **(SIE),** logic. Externally the transceiver connects to the physical layer of the USB.

4.9 PLL Clock Generator

A 48-MHz external crystal can be used with the SL811S/T. Two pins, X1 and X2, are provided to connect a low cost crystal circuit to the device (refer to *Figure 4-1*). If an external 48-MHz clock source is available in the application, it may be used instead of the crystal circuit by connecting directly to the X1 input pin.

The SL811S/T contains a built-in DPLL and 4X Clock Multiplier, which can be enabled by setting a register bit and driving the CM pin high, which allows operation with a 12 Mhz crystal or clock source. A suggested crystal circuit is shown in *Figure 4-2*.

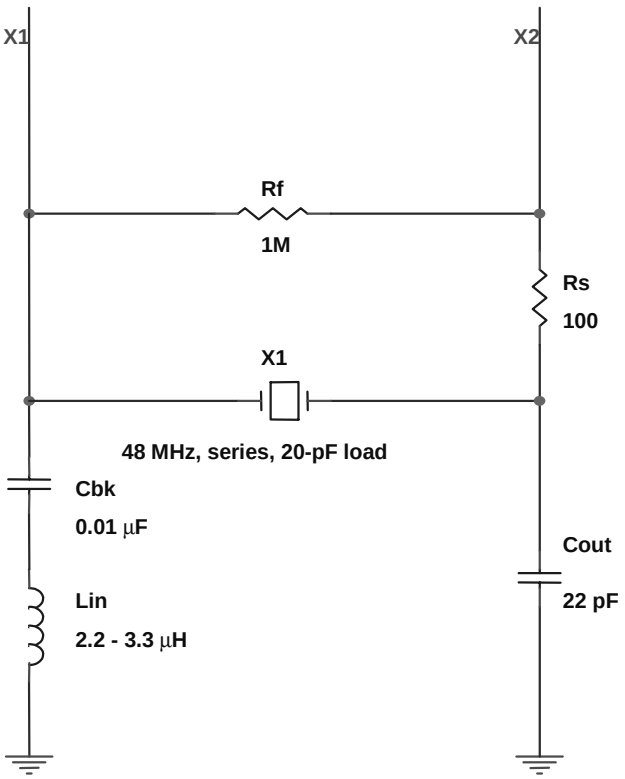


Figure 4-1. 48-MHz Crystal Circuit

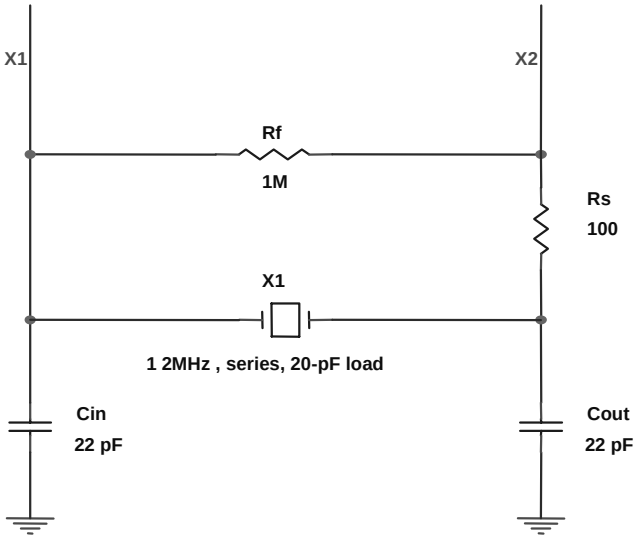


Figure 4-2. 12-MHz Crystal Circuit.

4.10 Power Resume and Suspend Mode

SL811S/T has a built-in SOF (Start of Frame) Detect Interrupt signal that can be monitored by an external microprocessor. The SOF indicates continuous USB activity and is transmitted by the USB Host every 1 ms (millisecond). The selected processor can use its timer to track non-SOFs or non-USB activity, and thus start the power Suspend sequence. The peripheral requires additional hardware to enable power shutdown to the SL811S/T, the removal of 3.3V power to USB Data+ line pull-up resistor, (which signals a disconnect t the USB Host), and to turn-off the clock to the SL811S/T. In Suspend mode, the unit will draw less than 40 µA (Micro-Amperes).

The SL811S/T can signal a wake-up to the Host USB device, providing the Pull-up resistor remains powered during the Suspend time. A register control bit allows the SL811S/T to output a 'K' State on the USB to signal the Host. See Force Function description in the Control Register Section. If the pull-up is powered down during Suspend, restoring power to the pull-up will signal a device connect to the USB host.

4.11 SL811S/T Registers

Operation and control of the SL811S/T is managed through the internal registers. A portion of the internal RAM is devoted to the register space and access is through the microprocessor interface. The registers provide control and status information for transactions on the USB, microprocessor interface, DMA and interrupts.

4.12 Auto Address Increment Mode

The SL811S/T supports auto increment mode to reduce read and write memory cycles. In this mode, the microcontroller needs to set up the address only once. Whenever any subsequent DATA is accessed, the internal address counter will advance to the next address location.

Once the address of the starting location has been set, the write operations will write the data bytes in consecutive locations. For example, assume the value Index1 was written into the Address register of SL811S/T during the Address cycle (with the A0 input set low). The write operations in the data cycle (with A0 input set High) will write the data bytes into the sequential internal memory locations Index1, Index1 + 1, Index1 + 2 and so on. The Auto increment mode also works on read operations from SL811S/T operations. After setting the address of the starting location once, the read operations will read the subsequent internal memory locations.

For example

Write 0x10 to SL811S/T in address cycle (A0 is set low)

Write 0x55 to SL811S/T in data cycle (A0 is set high) -> write 0x55 to location 0x10

Write 0xaa to SL811S/T in data cycle (A0 is set high) -> write 0xaa to location 0x11

Write 0xbb to SL811S/T in data cycle (A0 is set high) -> write 0xbb to location 0x12

Auto increment mode decreases the total time needed to transfer the block of data to or from the internal memory of the SL811S/T controller, eliminating the need to set the address for each byte to be transferred. The advantage of this mode is that it reduces the memory read or write cycles.

Please note when using some C Compilers, The Auto Increment mode may not work since some code implementations will generate low level code causing read-modify-write cycles. This will result in address errors.

5.0 SL811S/T Registers

The registers in the SL811S/T are divided into two major groups. The first group contains Endpoint Registers that manage USB control transactions and data flow. The second group contains the USB Registers that provide the control and status information for all other operations.

5.1 Endpoint Registers

Communication and data flow on the USB is implemented using endpoints. These uniquely identifiable entities are the terminals of communication flow between a USB host and USB devices. Each USB device is composed of a collection of independently operating endpoints. Each endpoint has a unique identifier, which is the Endpoint Number. For more information, see USB Specification 1.1 section 5.3.1.

The SL811S/T supports 4 endpoints numbered 0–3. Endpoint 0 is the default pipe and is used to initialize and generically manipulate the device to configure the logical device as the Default Control Pipe. It also provides access to the device's configuration information, allows USB status and control access, and supports control transfers.

Endpoints 1–3 support Bulk or Isochronous data transfers, and interrupts. Endpoint 3 is supported by DMA. Each endpoint has two sets of registers—the 'a' set and the 'b' set. This allows overlapped operation where one set of parameters is being set up and the other is transferring. Upon completion of a transfer to an endpoint, the 'next data set' bit indicates whether set 'a' or 'set 'b' will be in effect next. The 'armed' bit of the next data set will indicate whether the SL811S/T is ready for the next transfer without interruption.

5.2 Endpoints 0–3 Register Addresses

Each endpoint set has a group of five registers that are mapped within the SL811S/T memory. The register sets have address assignments as shown in the following table.

Endpoint Register Set	Address (in Hex)
Endpoint 0 – a	00 - 04
Endpoint 0 – b	08 - 0C
Endpoint 1 – a	10 - 14
Endpoint 1 – b	18 - 1C
Endpoint 2 – a	20 - 24
Endpoint 2 – b	28 - 2C
Endpoint 3 – a	30 - 34
Endpoint 3 – b	38 - 3C

For each endpoint set (starting at address Index = 0), the registers are mapped as shown in the following table:

Endpoint Register Sets (for Endpoint *n* starting at register position *Index=0*)	
Index	Endpoint *n* Control
Index + 1	Endpoint *n* Base Address
Index + 2	Endpoint *n* Base Length
Index + 3	Endpoint *n* Packet Status
Index + 4	Endpoint *n* Transfer Count

5.3 Endpoint Control Registers

Each endpoint set has a control register defined as follows:

Bit Position	Bit Name	Function
0	Arm	Allows enabled transfers when set =’1’. Clears to '0' when transfer is complete.
1	Enable	When set = '1' allows transfers to this endpoint. When set 0 USB transactions are ignored. If Enable = '1' and Arm = '0', the endpoint will return NAKs to USB transmissions.
2	Direction	When set = '1' transmit to Host. When '0', receive from Host.
3	Next Data Set	'0' if next data set is ‘a’, '1' if next data set is 'b'
4	ISO	When set to '1' allows Isochronous mode for this endpoint.
5	Send STALL	When set to ‘1’ sends Stall in response to next request on this endpoint.
6	Sequence	Sequence Bit. '0' if DATA0, '1' if DATA1.
7	Reserved	

5.3.1 Endpoint Base Address

Pointer to memory buffer location for USB reads and writes.

5.3.2 Endpoint Base Length

The Endpoint Base Length is the maximum packet size for Out transfers from the Host. Essentially, this designates the largest packet size that can be received by the SL811S/T. For Transfers In to Host, Base Length designates the size of the data packet to be sent.

5.3.3 Packet Status

The packet status contains information relative to the packet that has been received or transmitted. The register is defined as follows:

Bit Position	Bit Name	Function
0	ACK	Transmission Acknowledge.
1	Error	Error detected in transmission.
2	Time-out	Time-out occurred.
3	Sequence	Sequence Bit. '0' if DATA0, '1' if DATA1.
4	Setup	'1' indicates Setup Packet
5	Overflow	Overflow condition - maximum length exceeded during receives.
6	NAK	Slave returns NAK
7	STALL	Slave set STALL bit

5.3.4 Transfer Count

Contains the number of bytes left over (from ’Length’ field) after a packet is received. If an overflow condition occurs, i.e., the received packet from host was greater than the Length field, a bit is set in the Packet Status Register indicating the condition. The user can then determine the number of bytes received greater than the Length field specified by reading this register.

5.4 USB Control Registers

The USB Control registers manage communication and data flow on the USB. Each USB device is composed of a collection of independently operating endpoints. Each endpoint has a unique identifier, which is the Endpoint Number. For more details about USB endpoints, please refer to the USB Specification 1.1, Section 5.3.1.

The control and status registers are mapped as follows:

Register Name	Address (in Hex)
Control Register	05 h
Interrupt Enable Register	06 h
USB Address Register	07 h
Interrupt Status Register	0D h
Current Data Set Register	0E h
SOF Low Byte Register	15 h
SOF High Byte Register	16 h
DMA Total Count Low Byte Register	35 h
DMA Total Count High Byte Register	36 h

5.4.1 Control Register, Address [05H]

The Control Register enables/disables USB transfers and DMA Operations with control bits.

Bit Position	Bit Name	Function
0	USB Enable	Overall Enable for transfers. '1' enables, '0' disables.
1	DMA Enable	Enable DMA Operation when ‘1’. Disable = ‘0’.
2	DMA Dir	DMA transfer direction bit. Set ‘1’ for DMA read cycles from SL811S, Set ‘0’ for DMA write cycles.
3	J-K0	J-K Force State Bit 0. [See Force State Table]
4	J-K1	J-K Force State Bit 1.
5	SPSEL	Speed Select. ‘0’ select FS. ‘1’ select LS
6	STBYD	XCVR Power control. ‘1’ sets XCVR to low power. Normally ‘0’. Suspend mode is entered if Bit 6 is set = ‘1’ and Bit 0 (USB Enable) is set = ‘0’.
7	Reserved	Reserved bit - must be set to '0'.

Bit 0 should be set to ‘1’ to enable USB communication. The default is zero on power up.

Bit 1 is a DMA enable bit. DMA is initiated when DMA Count High is written.

Bit 2 sets the direction for DMA transfer.

Bits 3 – 4. The J-K force state control bits can be used to generate various USB bus conditions. Forcing K-state can be used for Peripheral device remote wake-up, Resume and other modes. These two bits are set to zero on power up.

JK-Force State	USB Engine Reset	Function
0	0	Normal operating mode
0	1	Force SE0, D+ and D– are set low
1	0	Force K-State, D– set high, D+ set low
1	1	Force J-State, D+ set high, Dq– set low

Bit 5. USB Speed select. ‘0’ sets the USB Speed for Full Speed (12 MHz). ‘1’ sets the USB for Low Speed 1.5 MHz operation.

Bit 6. ‘1’ sets the USB Transceiver for low power operation. Suspend Mode (Low power operation) is entered when Bit 6 is set = ‘1’ and Bit 0 (USB Enable) is set = ‘0’.

5.4.2 Interrupt Enable Register, Address [06h]

The SL811S/T provides an Interrupt Request Output that is activated resulting from a number of conditions. The Interrupt Enable Register allows the user to select activities that will generate the Interrupt Request. A separate Interrupt Status Register is provided. It can be read in order to determine the condition that initiated the interrupt. (See Interrupt Status Register description). When a bit is set to '1', the corresponding interrupt is enabled.

Bit Position	Bit Name	Function
0	Endpoint 0 Done	Enable Endpoint 0 done Interrupt
1	Endpoint 1 Done	Enable Endpoint 1 done Interrupt
2	Endpoint 2 Done	Enable Endpoint 2 done Interrupt
3	Endpoint 3 Done	Enable Endpoint 3 done Interrupt
4	DMA Done	Enable DMA done Interrupt
5	SOF Received	Enable SOF Received Interrupt
6	USB Reset	Enable USB Reset received interrupt.
7	DMA Status	When “1”, indicates DMA transfer in progress; When “0”, indicates DMA transfer is complete.*

5.4.3 USB Address Register, Address [07h]

Contains USB Device Address after assignment by USB Host during configuration. On power up or Reset, USB Address Register is set to Address 00H. After USB configuration and address assignment, the device will recognize only USB transactions directed to the address contained in the USB Address Register.

5.4.4 Interrupt Status Register, Address [0Dh]

This Read/Write register serves as an Interrupt status register when it is read, and an Interrupt clear register when it is written. To clear an interrupt bit, the register must be written with the appropriate bit set to '1'. Writing a '0' has no effect on the status.

Bit Position	Bit Name	Function
0	Endpoint 0 Done	Endpoint 0 done Interrupt
1	Endpoint 1 Done	Endpoint 1 done Interrupt
2	Endpoint 2 Done	Endpoint 2 done Interrupt
3	Endpoint 3 Done	Endpoint 3 done Interrupt
4	DMA Done	DMA done Interrupt
5	SOF Received	SOF Received Interrupt
6	USB Reset	USB Reset received interrupt.
7	DMA Status	When “1”, indicates DMA transfer in progress; When “0”, indicates DMA transfer is complete. An interrupt is not generated when DMA is complete.

5.4.5 Current Data Set Register, Address [0EH]

Register indicates currently selected data set for each endpoint.

Bit Position	Bit Name	Function
0	Endpoint 0	Endpoint 0a = 0, Endpoint 0b = 1
1	Endpoint 1	Endpoint 1a = 0, Endpoint 1b = 1
2	Endpoint 2	Endpoint 2a = 0, Endpoint 2b = 1
3	Endpoint 3	Endpoint 3a = 0, Endpoint 3b = 1
4-7	Reserved	For the Host

5.4.6 SOF Low Register, Address [15h]

Read only Register contains the 7 low order bits of Frame Number in positions: bit 7–1. Bit 0 is undefined. Register is updated when a SOF packet is received. User should not write to this register.

5.4.7 SOF High Register, Address [16h]

Read only Register contains the 4 low order bits of Frame Number in positions: bit 7–4. Bits 3–0 are undefined, and should be masked when read by the user. Register is updated when a SOF packet is received. User should not write to this register.

5.4.8 DMA Total Count Low Register, Address [35h]

Register contains the low order 8-bits of **DMA** count. **DMA** total count is the total number of bytes to be transferred between a peripheral to the SL811S/T. The count may sometimes require up to 16-bits, thus the count is represented in two registers: Total Count Low, and Total Count High. EP3 is only supported with DMA operation.

5.4.9 DMA Total Count High Register, Address [36h]

Register contains the High order 8-bits of **DMA** count. **When written, this register enables DMA** if the DMA Enable bit is set in the Control Register. User should always write Low Count Register first, followed by a write to High Count Register even if high count is 00H.

6.0 SL811S/T Physical Connection

The diagram below indicates the pin assignments for the SL811S 28-pin PLCC Package.

6.1 Pin Layout

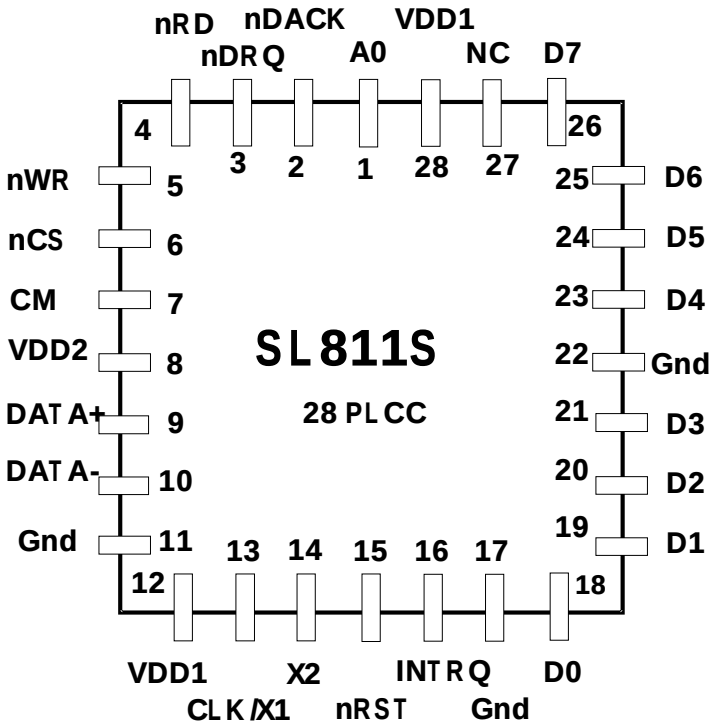
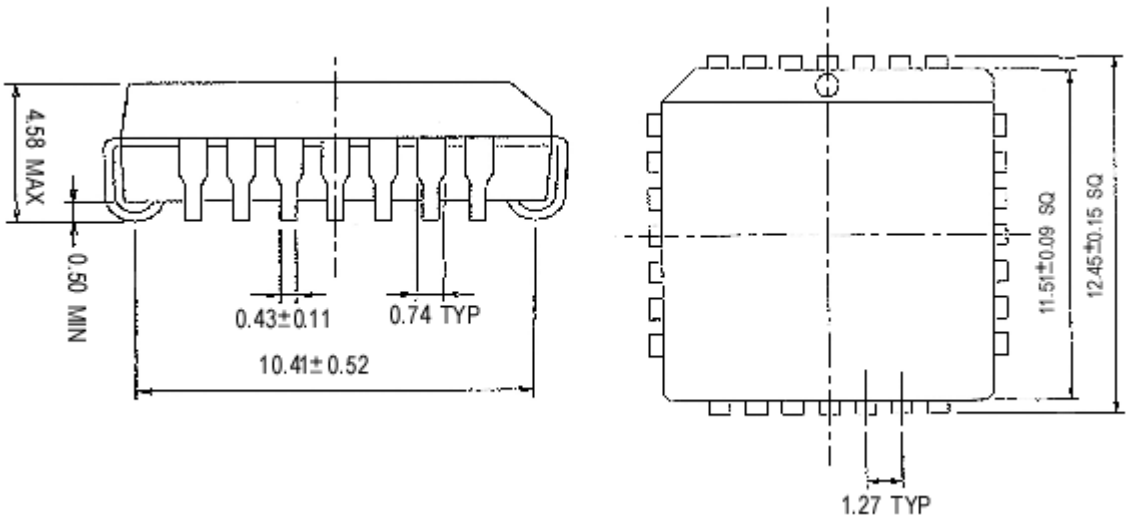


Figure 6-1. SL811S USB Controller—Pin layout

6.2 28-PIN PLCC Mechanical Dimensions



6.3 SL811S USB Controller, Pin Descriptions

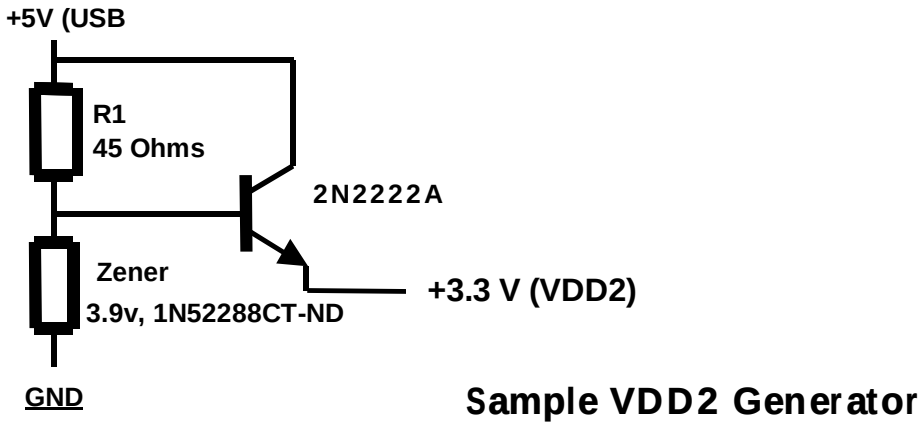
The SL811S package is a 28-pin PLCC. The device requires a 3.3VDC and a +3.3 VDC (VDD2) power supply for the USB transceiver. The SL811S requires an external 12 or 48 MHz crystal or Clock.

Pin No.	Pin Type	Pin Name	Pin Description
1	IN	A0	A0 = '0'. Selects Address Pointer. Reg. Write Only.[1] A0 = '1'. Selects Data Buffer or Register. R/W. In Multiplexed address applications; A0 should be tied to VDD1.
2	IN	nDACK	DMA Acknowledge. An active low input used to interface to an external DMA controller.
3	OUT	nDRQ	DMA Request. An active low output used with an external DMA controller. nDRQ and nDACK form the handshake for DMA data transfers.
4	IN	NRD	Read Strobe Input. An active low input used with nCS to read registers/data memory.
5	IN	NWR	Write Strobe Input. An active low input used with nCS to write to registers/data memory.
6	IN	NCS	Active low SL811S Chip select. Used with nRD and nWD when accessing SL811S.
7	IN	CM	Clock Mode. Enables DPLL 4x Multiplier for use with 12-MHz Clock.
8	VDD2	3.3 VDC	Power for USB Transceivers. Can be connected to Vdd1.
9	BIDIR	DATA +	USB Differential Data Signal High Side.
10	BIDIR	DATA -	USB Differential Data Signal Low Side.
11	GND	USB GND	Ground Connection for USB.
12	VDD1	3.3 VDC	SL811S Device VDD Power.
13	IN	CLK/X1	12/48 MHz Clock or External Crystal X1 connection.
14	OUT	X2	External Crystal X2 connection.
15	IN	NRST	SL811S Device active low reset input.
16	OUT	INTR	Active high Interrupt Request output to external controller.
17	GND	GND	SL811S Device Ground
18	BIDIR	D0	Data 0. Microprocessor Data/(Address) Bus.
19	BIDIR	D1	Data 1. Microprocessor Data/(Address) Bus.
20	BIDIR	D2	Data 2. Microprocessor Data/(Address) Bus.
21	BIDIR	D3	Data 3. Microprocessor Data/(Address) Bus.
22	GND	GND	SL811S Device Ground.
23	BIDIR	D4	Data 4. Microprocessor Data/(Address) Bus.
24	BIDIR	D5	Data 5. Microprocessor Data/(Address) Bus.
25	BIDIR	D6	Data 6. Microprocessor Data/(Address) Bus.
26	BIDIR	D7	Data 7. Microprocessor Data/(Address) Bus.
27	NC	NC	No Connect.
28	VDD1	3.3 VDC	SL811S Device VDD Power.

Notes:

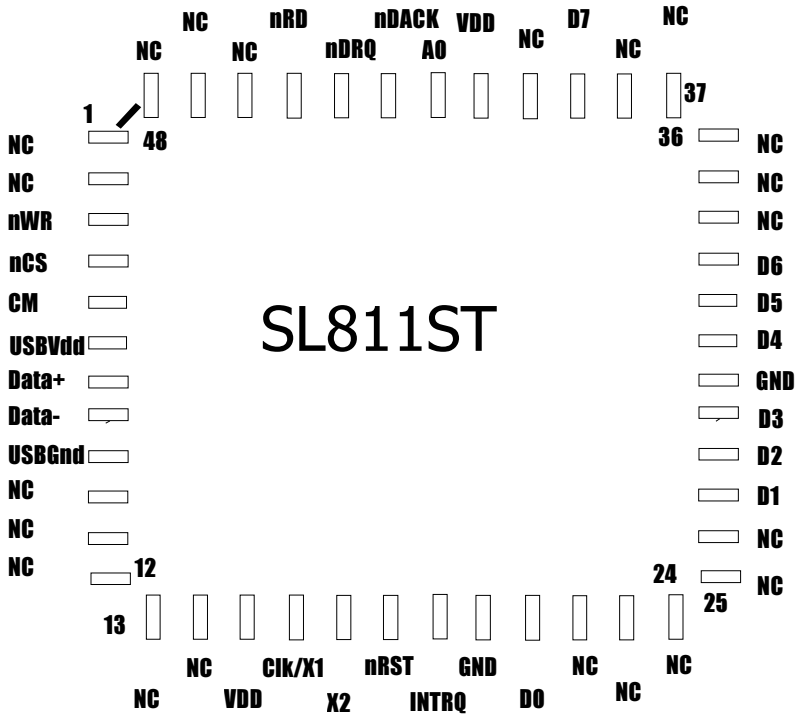
1. The A0 Address bit is used to access the address register or data registers in I/O Mapped or Memory Mapped applications.
2. VDD2 can be derived from a +5 VDC supply with a few additional components. The diagram below illustrates a simple method that provides 3.3V/22 mA. Another option is to use a Torex Semiconductor 3.3V SMD regulator P/N XC62HR3302MR.
3. X1/X2 Clock requires external 12-/48-MHz matching crystal or clock source.

A simple 3.3V voltage source

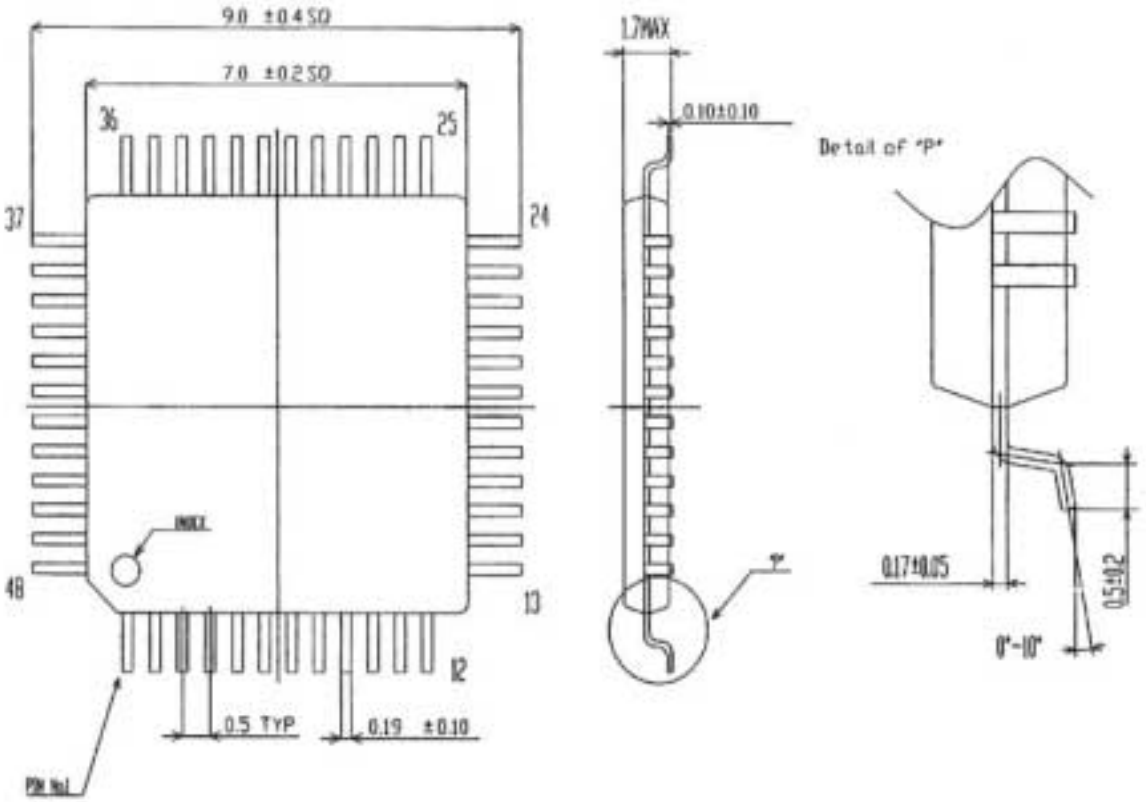


6.4 SL811ST Pin Layout

The diagram below shows the pin assignments for SL811ST 48-pin LPQFP Package.



6.5 SL811ST 48-Pin LPQFP Mechanical Dimensions



6.6 SL811ST USB Controller, Pin Descriptions

The SL811ST is packaged in a 48-Pin LPQFP. The device requires 3.3VDC or +5VDC (VDD1) and a +3.3 VDC (VDD2) power supply. Average typical current consumption is less than 22 mA for 3.3 V. The SL811ST requires an external 48-MHz Crystal or Clock.

Pin No.	Pin Type	Pin Name	Pin Description
1	NC	NC	NC
2	NC	NC	NC
3	IN	nWR	Write Strobe Input. An active low input used with nCS to write to registers/data memory.
4	IN	nCS	Active low SL811ST Chip select. Used with nRD and nWR when accessing SL811ST.
5	IN	CM	Clock Mode. Enables DPLL 4x Multiplier when ‘1’. For use with 12-MHz Clock. Tie to gnd for 48-MHz.
6	VDD2	3.3 VDC	Power for USB Transceivers. VDD2 may be derived from VDD1. **Note 4???**
7	BIDIR	DATA+	USB Differential Data Signal High Side.
8	BIDIR	DATA–	USB Differential Data Signal Low Side.
9	GND	USB GND	Ground Connection for USB.
10	NC	NC	NC
11	NC	NC	NC

Pin No.	Pin Type	Pin Name	Pin Description
12	NC	NC	NC
13	NC	NC	NC
14	NC	NC	NC
15	VDD1	3.3 VDC	SL811ST Device VDD Power.
16	IN	CLK/X1	12/48 MHz Clock or External Crystal X1 connection.
17	OUT	X2	External Crystal X2 connection.
18	IN	nRST	SL811ST Device active low reset input.
19	OUT	INTRQ	Active High Interrupt Request output to external controller.
20	GND	GND	SL811ST Device Ground.
21	BIDIR	D0	Data 0. Microprocessor Data/(Address) Bus.
22	NC	NC	NC
23	NC	NC	NC
24	NC	NC	NC
25	NC	NC	NC
26	NC	NC	NC
27	BIDIR	D1	Data 1. Microprocessor Data/(Address) Bus.
28	BIDIR	D2	Data 2. Microprocessor Data/(Address) Bus.
29	BIDIR	D3	Data 3. Microprocessor Data/(Address) Bus.
30	GND	GND	SL811ST Device Ground.
31	BIDIR	D4	Data 4. Microprocessor Data/(Address) Bus.
32	BIDIR	D5	Data 5. Microprocessor Data/(Address) Bus.
33	BIDIR	D6	Data 6. Microprocessor Data/(Address) Bus.
34	NC	NC	NC
35	NC	NC	NC
36	NC	NC	NC
37	NC	NC	NC
38	NC	NC	NC
39	BIDIR	D7	Data 7. Microprocessor Data/(Address) Bus.
40	NC	NC	NC.
41	VDD1	3.3 VDC	SL811ST Device VDD Power.
42	IN	A0	A0 = ’0’. Selects Addr. Pointer. Reg. Write Only. Note 1 A0 = ’1’. Selects Data Buffer or Register.
43	IN	nDACK	DMA Acknowledge. An active low input used to interface to an external DMA controller.
44	OUT	nDRQ	DMA Request. An active low output used with an external DMA controller. nDRQ and nDACK form the handshake for DMA data transfers.
45	IN	nRD	Read Strobe Input. An active low input used with nCS to read registers/data memory.
46	NC	NC	NC
47	NC	NC	NC
48	NC	NC	NC

7.0 Electrical Specifications

7.1 Absolute Maximum Ratings

This section lists the absolute maximum ratings of the SL811S. Stresses above those listed can cause permanent damage to the device. Exposure to maximum rated conditions for extended periods can affect device operation and reliability.

Storage Temperature	–40 to 125 °C
Voltage on any pin with respect to ground	–0.3 V 6.0 V
Power Supply Voltage (VDD)	3.3 V ±10%
Power Supply Voltage (USBVDD)	3.3 V ±10%
Lead Temperature (10 seconds)	180°C

7.1.1 Recommended Operating Condition

Parameter	Min.	Typical	Max.
Power Supply Voltage, VDD	3.0V	3.3V	3.6V
Power Supply Voltage, USBVDD	3.0V		3.6V
Operating Temperature	0°C		65°C

7.1.2 Crystal Requirement

Crystal Requirements, (X1, X2)	Min.	Typical	Max.
Operating Temperature Range	0°C		65°C
Series Resonant Frequency[4]		48 MHz	
Frequency Drift over Temperature			±100 ppm
Accuracy of Adjustment			±100 ppm
Series Resistance			100 ohms
Shunt Capacitance	3 pF		6 pF
Load Capacitance		20 pF	
Drive Level	20 µW		5 mW
Mode of Vibration 3rd overtone			

Note:
4. The SL811 can also use a 12-MHz Crystal Oscillator or 12-MHz Clock Source.

7.2 External Clock Input Characteristics (48 MHz) (X1)

Parameter	Min.	Typical	Max.
Clock Input Voltage @ X1 (X2 Open)	1.5V		
Clock Frequency		48 MHz	

7.3 DC Characteristics

Parameter	Description	Min.	Typical	Max.
V_{IL}	Input Voltage LOW	–0.3V		0.8V
V_{IH}	Input Voltage HIGH (5V Tolerant I/O)	2.0V		6.0V
V_{OL}	Output Voltage LOW (I_{OL} = 4 mA)			0.4V
V_{OH}	Output Voltage HIGH (I_{OH} = –4 mA)	2.4V		
I_{OH}	Output Current HIGH	4 mA		
I_{OL}	Output Current LOW	4 mA		
I_{LL}	Input Leakage			±1 µA
C_{IN}	Input Capacitance			10 pF
I_{CC}[5]	Supply Current (VDD) inc USB @FS		21 mA	25 mA
I_{CCsus1}[6]	Supply Current (VDD) Suspend w/Clk & Pll Enb		4.2 mA	5 mA
I_{CCsus2}[7]	Supply Current (VDD) Suspend no Clk & Pll Dis.		50 µA	60 µA
I_{USB}	Supply Current (VDD1)			10 mA
I_{USBSUS}	Transceiver Supply Current in Suspend			10 µA

7.4 USB Transceiver Characteristics

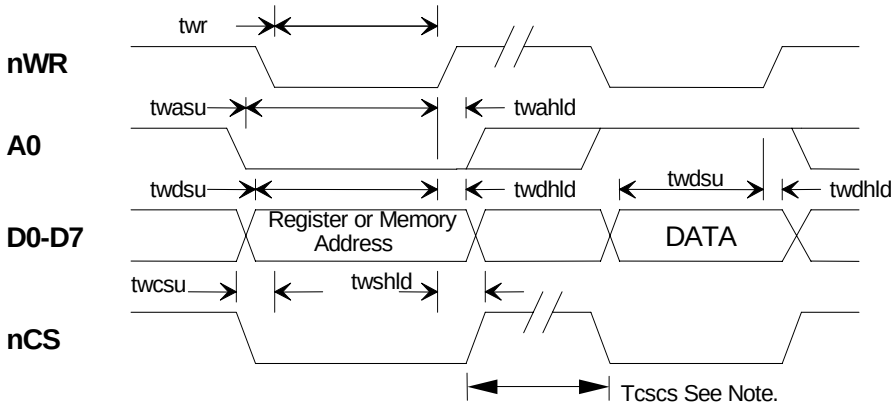
Parameter	Description	Min.	Typical[8]	Max.
V_{IHYS}	Differential Input Sensitivity (D+, D–)	0.2V		
V_{USBIH}	USB Input Voltage HIGH Driven	2.0V		
V_{USBIL}	USB Input Voltage LOW			0.8V
V_{USBOH}	USB Output Voltage HIGH	2.8V		
V_{USBOL}	USB Output Voltage LOW	0.0V		0.3V
Z_{USBH}[9]	Output Impedance HIGH STATE	33 Ohms		42 Ohms
Z_{USBL}[9]	Output Impedance LOW STATE	33 Ohms		42 Ohms
I_{USB}	Transceiver Supply p-p Current (3.3V)			10 mA At Full Speed.
I_{USBSUS}	Transceiver Supply Current in Suspend			10 µA

Notes:

5. I_{CC} measurement includes USB Transceiver current operating at Full Speed.
6. I_{CCSUS1} measured with 12-MHz Clock Input and Internal PLL enabled. Suspend set –(USB transceiver and internal Clocking disabled).
7. I_{CCSUS2} measured with external Clock and PLL disabled and Suspend set. For absolute minimum current consumption ensure that all inputs to the device are at static logic level.
8. All typical values are VDD = 3.3V and Tamb= 25°C.
9. Z_{USBX} Impedance Values includes an external resistor of 33–42 Ohms ±1%.

7.5 Bus Interface Timing Requirements

7.5.1 I/O Write Cycle



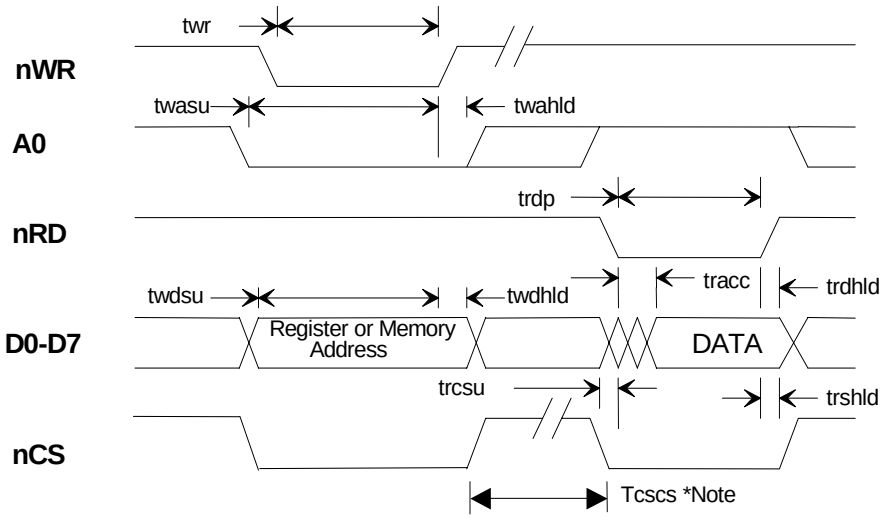
I/O Write Cycle to Register or Memory Buffer

Note: nCS can be held low for multiple write cycles provided nWR is cycled.

Parameter	Description	Min.	Typical	Max.
twr	Write pulse width	65 ns		
twcsu	Chip select set-up to nWR	0 ns		
twshld	Chip select hold time	0 ns		
twasu	A0 address set-up time	65 ns		
twahld	A0 address hold time	10 ns		
twdsu	Data to write low set-up time	60 ns		
twdhld	Data hold time after write high	5 ns		
tcscs	nCS inactive to nCS[10] asserted	85 ns[10]		

Note:
10. I/O Write Cycle Time in Auto Inc Mode is 150 ns minimum.

7.5.2 I/O Read Cycle

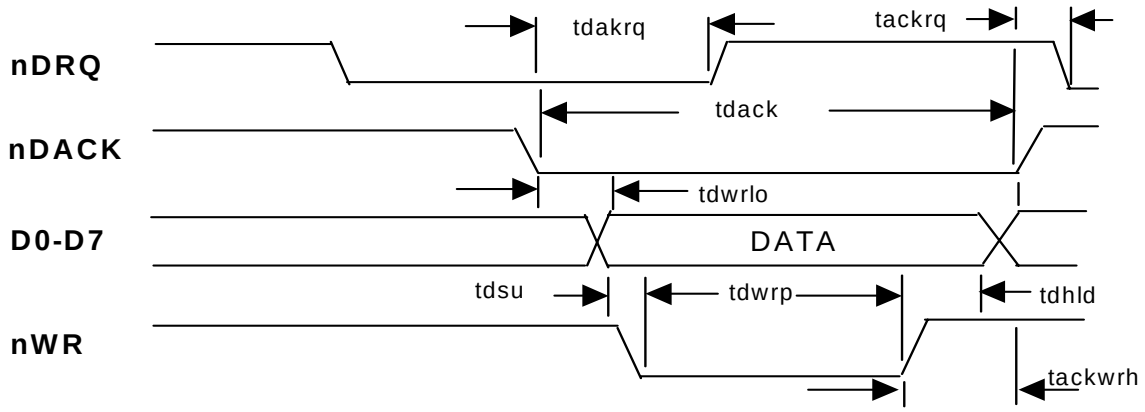


I/O Read Cycle from Register or Memory Buffer

Parameter	Description	Min.	Typical	Max.
twr	Write pulse width	65 ns		
trd	Read pulse width	65 ns		
twcsu	Chip select set-up to nWR	0 ns		
twasu	A0 address set-up time	65 ns		
twahld	A0 address hold time	10 ns		
twdsu	Data to write high set-up time	10 ns		
twdhld	Data hold time after write high	5 ns		
tracc	Data valid after read low	20 ns		25 ns
trdhld	Data hold after read high	5 ns		
trcsu	Chip select low to read low	0 ns		
trshld	Chip select hold after read high	0 ns		
Tcscs[11]	nCS inactive to nCS asserted[11]	85 ns		

Note:
11. nCS can be held low for multiple Read cycles providing the nRD line is cycled. I/O Write Cycle Time in Auto Inc Mode is 150 ns minimum.

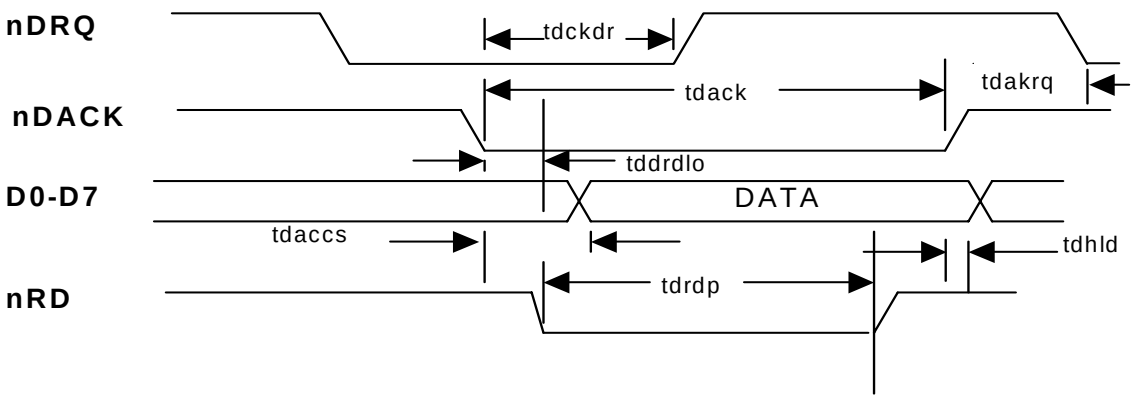
7.5.3 SL811S DMA Write Cycle



Parameter	Description	Min.	Typ.	Max.
tdack	nDACK low	80ns		
tdwrlo	nDACK to nWR low delay	5 ns		
tdakrq	nDACK low to nDRQ high delay	5 ns		
tdwrp	nWR pulse width	65 ns		
tdhld	Data hold after nWR high	5 ns		
tdsu	Data set-up to nWR strobe low	60 ns		
tackrq	NDACK high to nDRQ low	5 ns		
tackwrh	NDACK high to nDRQ low	5 ns		
twrcycle	DMA Write Cycle Time	150 ns		

Note: n**WR** must go low after n**DACK** goes low in order for n**DRQ** to clear. If this sequence is not implemented as requested, the next n**DRQ** will be not inserted.

7.5.4 SL811S DMA Read Cycle

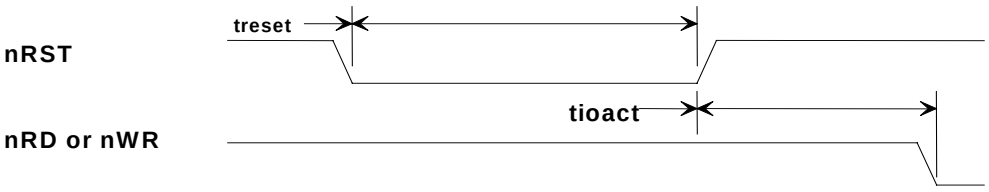


SL811 DMA READ CYCLE TIMING

Parameter	Description	Min.	Typ.	Max.
tdack	nDACK low	100 ns		
tddrdlo	nDACK to nRD low delay	0 ns		
tdckdr	nDACK low to nDRQ high delay	5 ns		
tdrdp	nRD pulse width	90 ns		
tdhld[12]	Date hold after nDACK high	5 ns		
tddaccs	Data access from nDACK low	85 ns		
tdrdack	nRD high to nDACK high	0 ns		
tdakrq	nDRQ low after nDACK high	5 ns		
trdcycle	DMA Read Cycle Time	150 ns		

Note:
12. Data is held until nDACK goes high regardless of state of nREAD.

7.5.5 Reset Timing

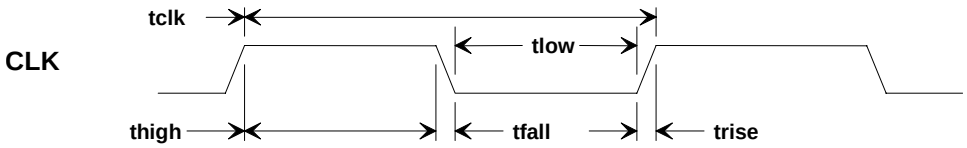


RESET TIMING

Parameter	Description	Min.	Typical	Max.
treset	nRst Pulse width	16 clocks		
tioact	nRst high to nRD or nWR active	16 clocks		

Note: Clock is 48 MHz nominal.

7.5.6 Clock Timing Specifications



CLOCK TIMING

Parameter	Description	Min.	Typical	Max.
tclk	Clock period (48 MHz)	20.0 ns	20.8 ns	
thigh	Clock high time	9 ns		11 ns
tlow	Clock low time	9 ns		11 ns
trise	Clock rise time			3 ns
tfall	Clock fall time			3 ns
	Clock Duty Cycle	45%		55%

8.0 Revision History

Document Title: SL811HS/T USB Dual Speed Slave Controller Data Sheet Document Number: 38-08009				
REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	110851	12/21/01	BHA	Converted to Cypress Format from ScanLogic