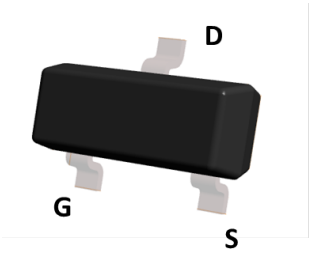
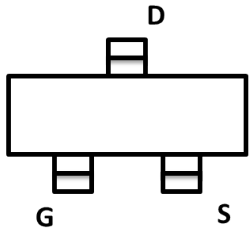
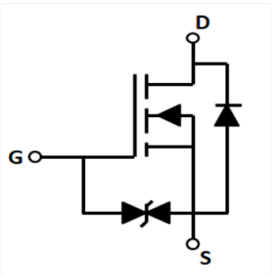
N-Channel Enhancement Mode Field Effect Transistor



Top View



SOT-23



Product Summary

- V_{DS} 20V
- I_D 7.0A
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜18 mohm
- $R_{DS(ON)}$(at V_{GS}=2.5V) ＜22 mohm
- $R_{DS(ON)}$(at V_{GS}=1.8V) ＜39 mohm
- ESD Protected Up to 3.0KV (HBM)

General Description

- Trench Power LV MOSFET technology
- High Power and current handing capability

Applications

- PWM application
- Load switch

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	20	V
Gate-source Voltage		V_{GS}	±12	V
Drain Current	T_A=25℃ @ Steady State	I_D	7.0	A
	T_A=70℃ @ Steady State		5.6	
Pulsed Drain Current [A]		I_{DM}	30	A
Total Power Dissipation @ T_A=25℃		P_D	1.3	W
Thermal Resistance Junction-to-Ambient		$R_{\theta JA}$	96	℃/ W
Thermal Resistance Junction-to-Lead @ Steady State		$R_{\theta JL}$	80	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL3416A	F2	8810.	3000	30000	120000	7“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±10V, V_{DS}=0V		2.5	±10	μA
		V_{GS}= ±8V, V_{DS}=0V		500	±2000	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	0.45	0.62	1.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 4.5V, I_D=7.0A		13	18	mΩ
		V_{GS}= 2.5V, I_D=4.0A		17	22	
		V_{GS}= 1.8V, I_D=1.5A		27	39	
Diode Forward Voltage	V_{SD}	I_S=7.0A,V_{GS}=0V			1.2	V
Maximum Body-Diode Continuous Current	I_S				7.0	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=10V,V_{GS}=0V,f=1MHZ		890		pF
Output Capacitance	C_{oss}			133		
Reverse Transfer Capacitance	C_{rss}			120		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=4.5V,V_{DS}=10V,I_D=7.0A		11		nC
Gate Source Charge	Q_{gs}			1.73		
Gate Drain Charge	Q_{gd}			3.1		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=4.5V,V_{DD}=10V, R_L=1.5Ω, R_{GEN}=3Ω		7		ns
Turn-on Rise Time	t_r			45		
Turn-off Delay Time	$t_{D(off)}$			30		
Turn-off Fall Time	t_f			52		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

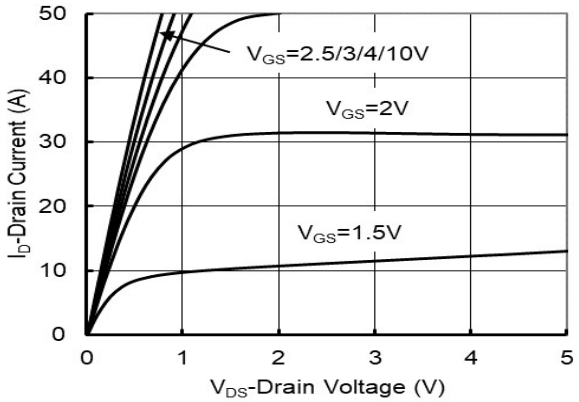


Figure1. Output Characteristics

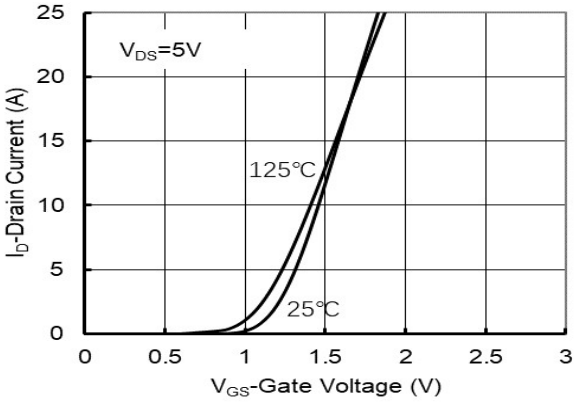


Figure2. Transfer Characteristics

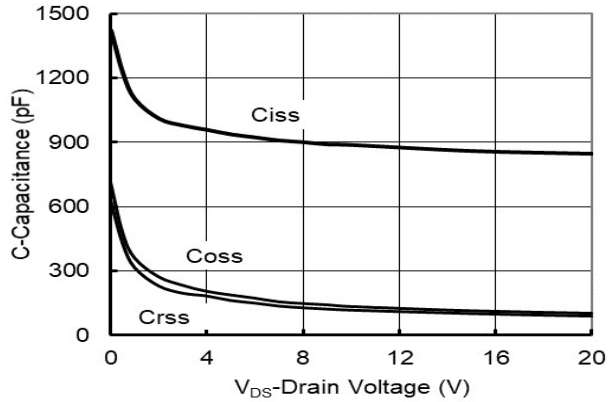


Figure3. Capacitance Characteristics

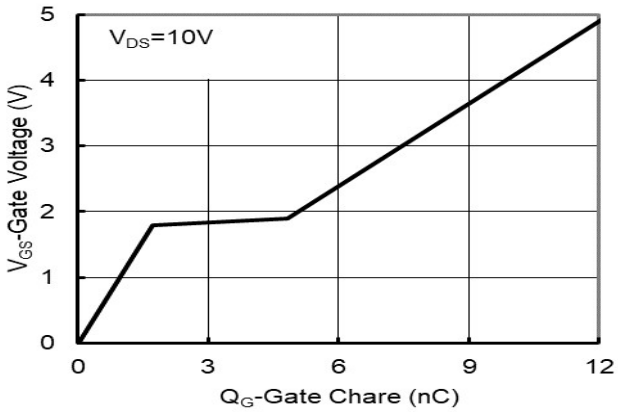


Figure4. Gate Charge

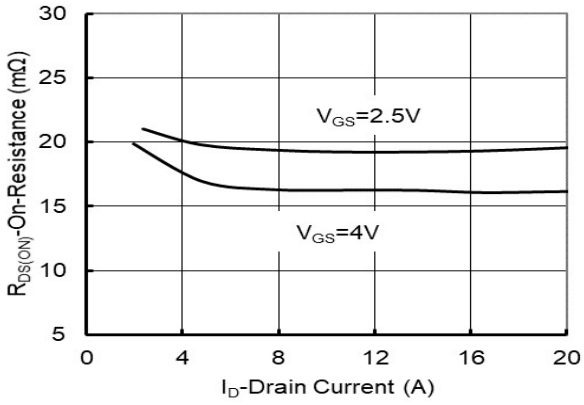


Figure5. Drain-Source on Resistance

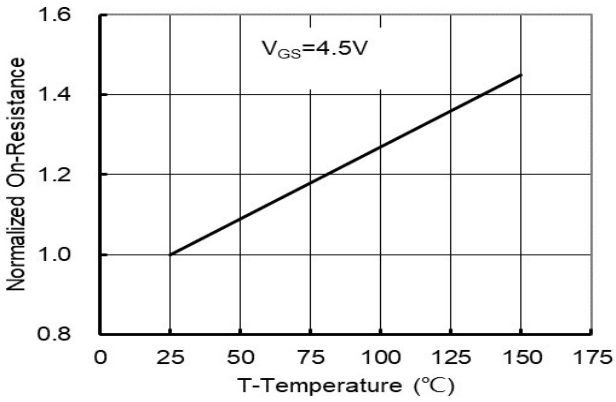


Figure6. Drain-Source on Resistance

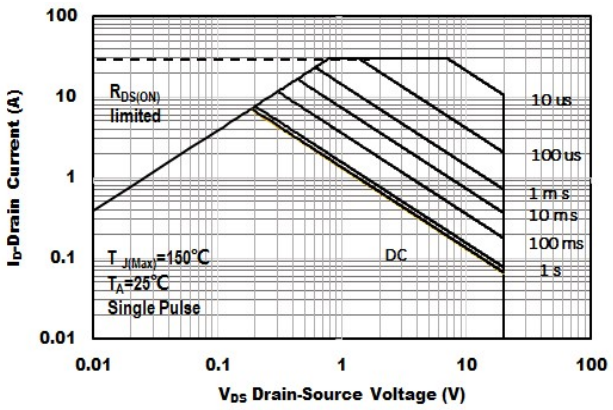


Figure7. Safe Operation Area

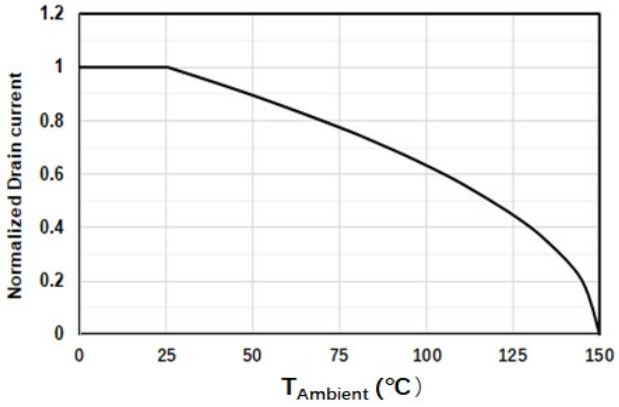


Figure8. Drain Current vs Ambient Temperature

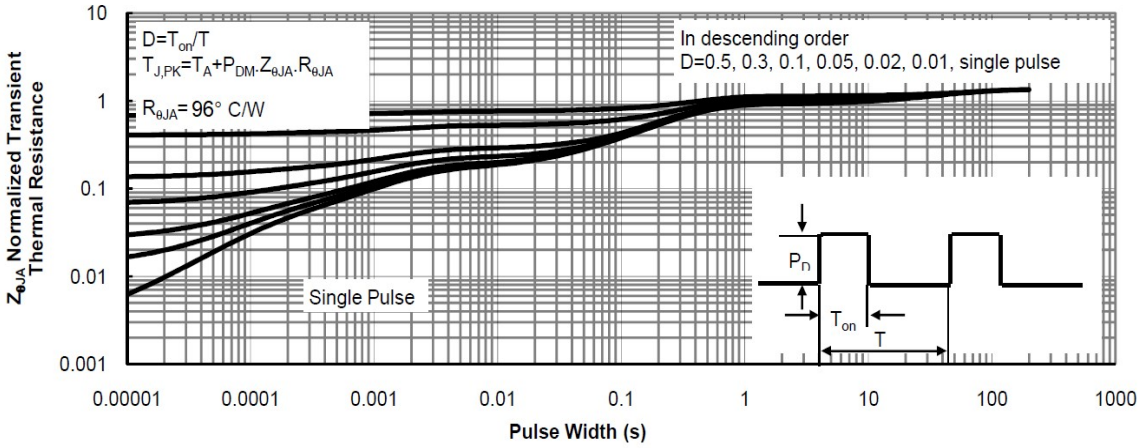
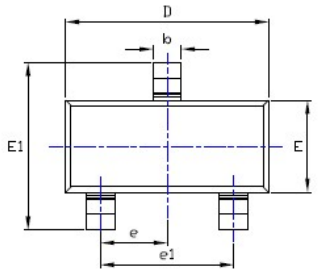
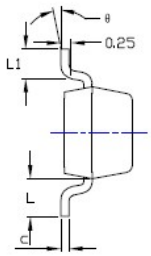


Figure9. Normalized Maximum Transient Thermal Impedance

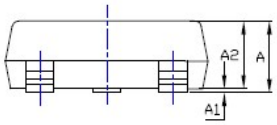
■SOT-23 Package information



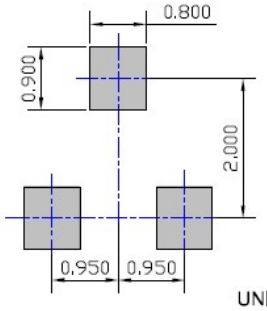
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT：mm

SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS						
SYMBOL	INCHES			Millmeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.035	---	0.045	0.900	---	1.150
A1	0.000	---	0.004	0.000	---	0.100
A2	0.035	0.038	0.041	0.900	0.975	1.050
b	0.012	0.016	0.020	0.300	0.400	0.500
c	0.004	---	0.008	0.100	---	0.200
D	0.110	0.114	0.118	2.800	2.900	3.000
E	0.047	0.051	0.055	1.200	1.300	1.400
E1	0.089	0.094	0.100	2.250	2.400	2.550
e	0.037TYP			0.950TYP		
e1	0.071	0.075	0.079	1.800	1.900	2.000
L	0.022REF			0.550REF		
L1	0.012	0.016	0.200	0.300	0.400	0.500
θ	0°	---	8°	0°	---	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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