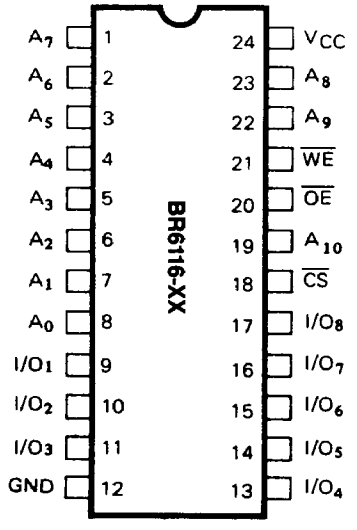
2K × 8 High Speed CMOS SRAM

Features

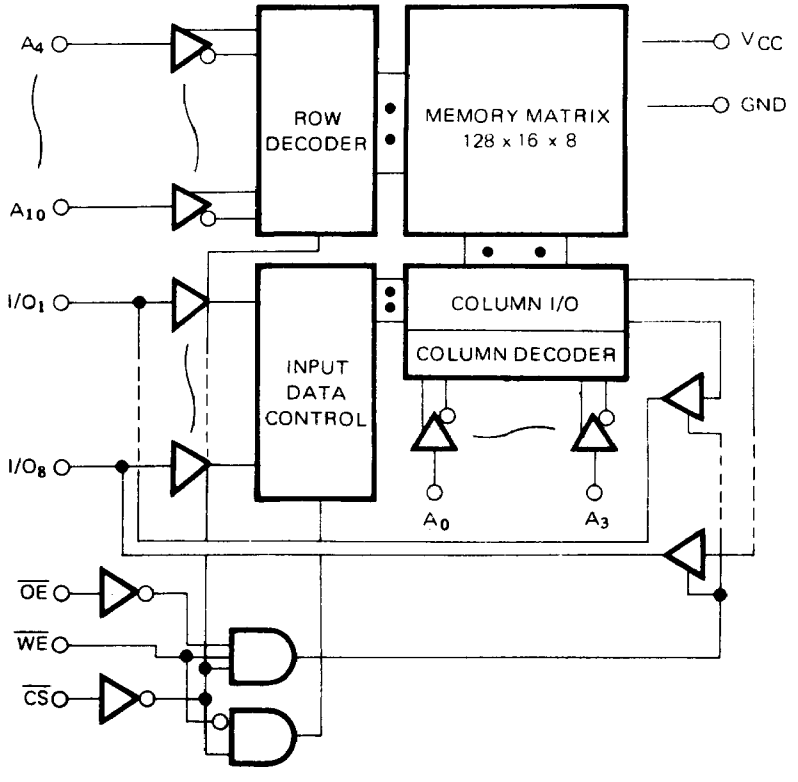
- Single 5V supply and high density 24 pin package
- High speed: Fast access time 90ns/120ns (max.)
- Low power standby 5μW (typ.)
  Low power operation 250mW (typ.)
- Completely static RAM: No Clock or timing strobe required
- Directly TTL compatible: All inputs and outputs
- Pin Compatible with standard 16K EPROM/Mask ROM
- Equal access and cycle time
- Package BR6116-09/-12 24 pin DIP (plastic)
  BR6116F-09/-12 24 pin SOP (plastic)

The BR6116 is a 16,384-bit static random access memory organized as 2048 words by 8 bits and operates from a single 5-volt supply. It is built with a high performance CMOS process. Six transistor full CMOS memory cell provides low standby current and high-reliability. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The BR6116 is available in a standard 24-pin 600mil-DIP and SO package.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Voltage on Any Pin Relative to GND, V_T . −0.3V to +7.0V
Operating Temperature, T_{opr} . . . . . 0°C to +70°C
Storage Temperature (Plastic), T_{stg} . . . −55°C to +125°C
Temperature Under Bias, T_{bias} . . . . . −10°C to +85°C
Power Dissipation, P_T 1.0W/Sop 0.7W
Soldering temp. & time . . . . . 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	x	x	Standby	I_{SB}, I_{SB1}	High Z
L	L	H	Read	I_{CC}	Dout
L	H	H	Output Disable	I_{CC}	High Z
L	x	L	Write	I_{CC}	Din

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	5.8	V
	V_{IL}	−0.3	−	0.8	V

DC and Operating Characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_A = 0 to +70°C)

Item	Symbol	Test Conditions	6116-09			6116-12			Units
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input Leakage Current	I_{LI}	V_{CC}=5.5V, V_{IN}=GND to V_{CC}	−	−	10	−	−	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	−	−	10	−	−	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	−	30	60	−	30	60	mA
	I_{CC1}	V_{IH} = 3.5V, V_{IL} = 0.6V, $I_{I/O}$ = 0mA	−	30	−	−	30	−	mA
Dynamic Operating Current	I_{CC2}	Min. Cycle, duty = 100%	−	−	100	−	−	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	−	0.5	1	−	0.5	1	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} −0.2V, V_{IN} ≥ V_{CC} −0.2V or V_{IN} ≤ 0.2V	−	1	100	−	1	50	μA
Output Voltage	V_{OL}	I_{OL} = 4mA	−	−	0.4	−	−	0.4	V
	V_{OH}	I_{OH} = −1.0mA	2.4	−	−	2.4	−	−	V

*V_{CC} = 5V, T_A = 25°C

A.C. Characteristics

(V_{CC} = 5V ± 10%, T_A = 0 to +70°C)

A.C. Test Conditions

Input Pulse Levels: 0V to 3.0V
Input Rise and Fall Times: 5ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

READ CYCLE

Item	Symbol	6116-09		6116-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	90	–	120	–	ns
Address Access Time	t_{AA}	–	90	–	120	ns
Chip Select Access Time	t_{ACS}	–	90	–	120	ns
Chip Selection to Output in Low Z	t_{CLZ}	5	–	10	–	ns
Output Enable to Output Valid	t_{OE}	–	50	–	50	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	10	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	40	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	40	ns
Output Hold from Address Change	t_{OH}	5	–	10	–	ns

WRITE CYCLE

Item	Symbol	6116-09		6116-12		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	90	–	120	–	ns
Chip Selection to End of Write	t_{CW}	55	–	70	–	ns
Address Valid to End of Write	t_{AW}	80	–	85	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	ns
Write Pulse Width	t_{WP}	55	–	70	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	40	ns
Write to Output in High Z	t_{WHZ}	0	50	0	50	ns
Data to Write Time Overlap	t_{DW}	30	–	35	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	ns
Output Active from End of Write	t_{OW}	0	–	5	–	ns

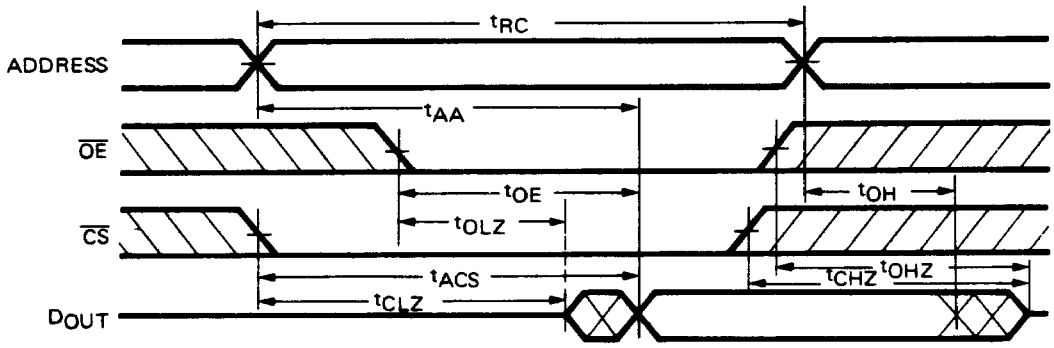
Capacitance* (f = 1MHz, T_A = 25°C)

Item	Symbol	Test Conditions	Max.	Unit
Input Capacitance	Cin	Vin = 0V	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	10	pF

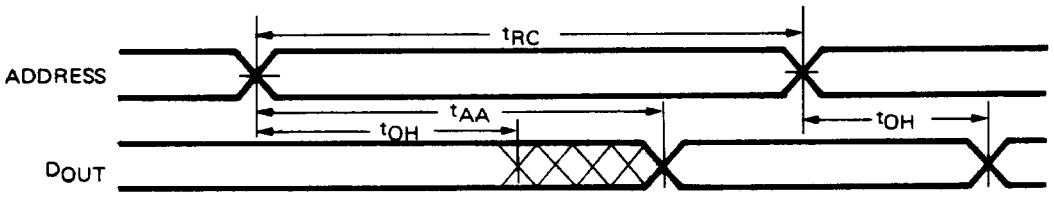
*This parameter is sampled and not 100% tested.

Timing Waveform

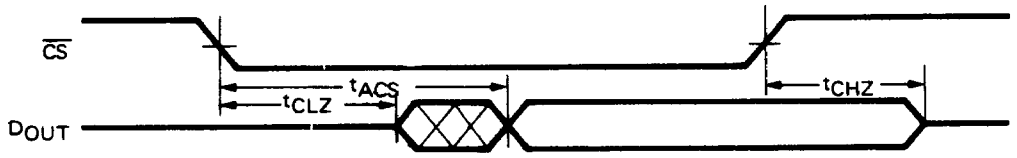
READ CYCLE (1)[1]



READ CYCLE (2)[1][2][4]

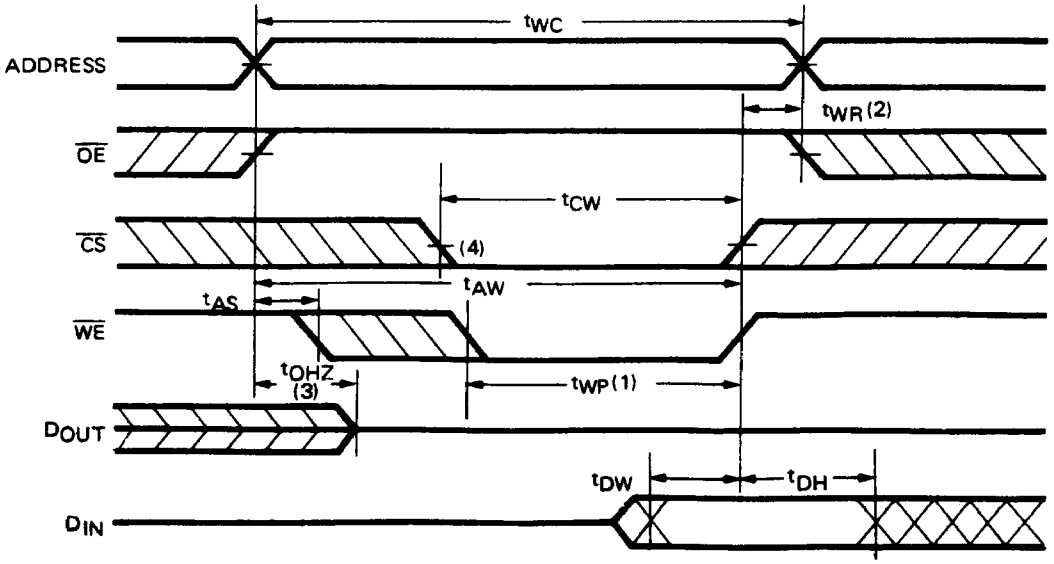


READ CYCLE (3)[1][3][4]

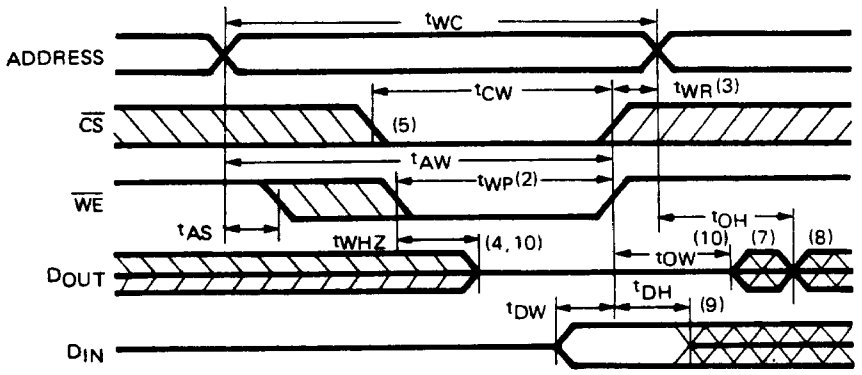


Notes:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.

WRITE CYCLE (1)



WRITE CYCLE (2) (1)(6)



Notes:

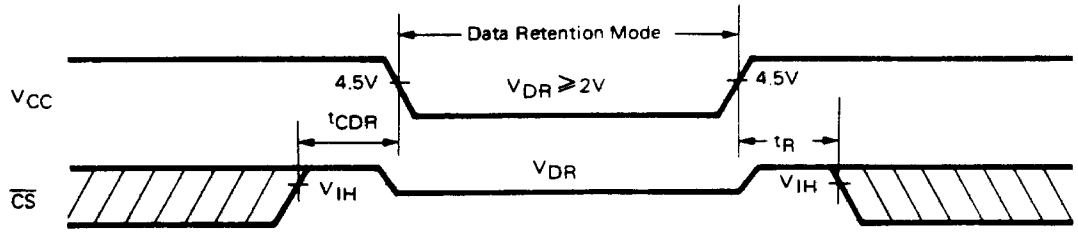
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.

Data Retention Characteristics over the operating temperature range

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
V_{DR}	V_{CC} for Retention Data	$\overline{CS} = V_{CC}$	2.0	–	–	V
I_{CCDR}	Data Retention Current	V_{IN} = 0V or V_{CC}	–	2	20	μA
t_{CDR}	Chip Deselect to Data Retention Time	V_{CC} = 2.0V, CS = V_{CC}	0	–	–	ns
t_R	Operation Recovery Time	V_{IN} = 0V or V_{CC}	t_{RC}(2)	–	–	ns

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform

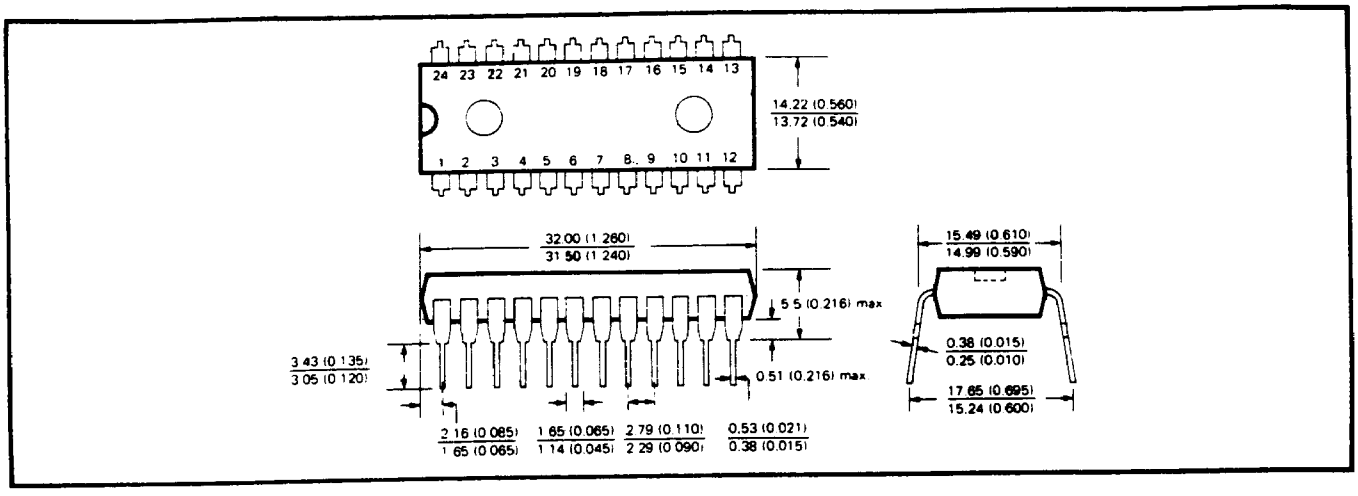


Ordering Information

Part Number	Access Time (Max.)	Package
BR6116-12	120 ns	Plastic 24-pin DIP
BR6116-09	90 ns	Plastic 24-pin DIP
BR6116F-12	120 ns	Plastic 24-pin SOP
BR6116F-09	90 ns	Plastic 24-pin SOP

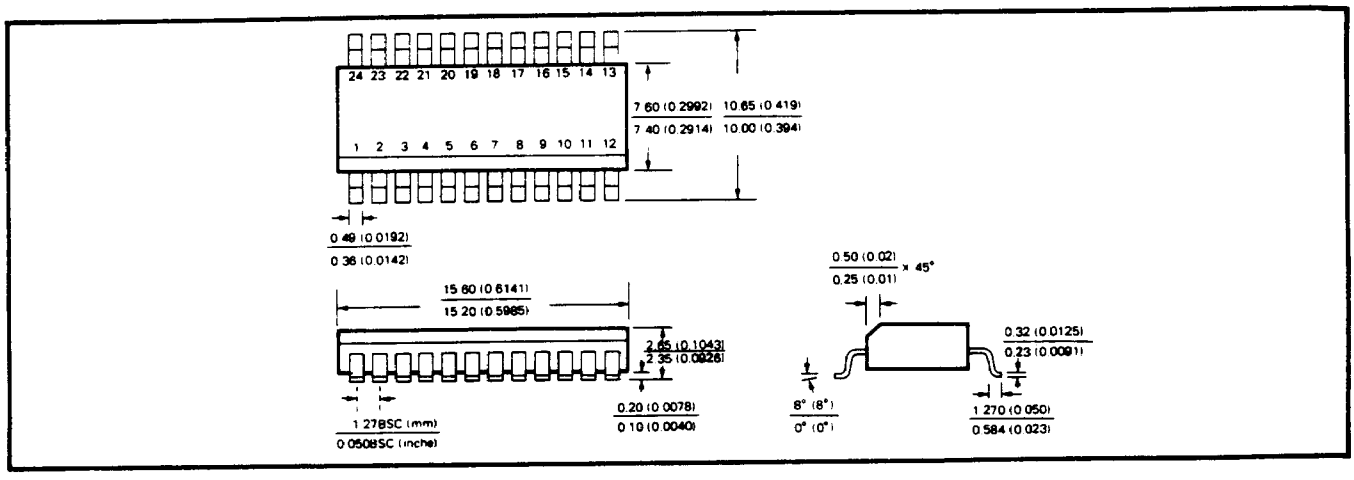
Package Information – mm (inch)

24-LEAD DUAL IN-LINE; PLASTIC



24-PIN SMALL OUTLINE

Unit: mm (inch)



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