Type	Silicon Monolithic Integrated Circuit
Product Name	Sound Generator for Cellular Phone
Product No.	BU8793KN
Physical Dimensions	Fig.1 Mechanical dimension
Block Diagram	Fig.2 Block diagram

Features

1) 16 harmonies generator available at the same time
   128 sounds + drum set 47 sounds generation
2) ADPCM decode functions are mounted, and mixing with sounds is possible
3) FIFO buffer and sequencer are used to reduce CPU load
4) RAM is mounted as FIFO buffer for down load data
5) 12.5~18MHz system clock available
6) Synchronization of text and LED is prepared
7) Stereo sound available
8) PitchBend and vibrato available
9) Integrated stereo sound DAC
10) Integrated secondary LPF (fc=20kHz) for smoothing
11) Power down mode is supported
12) CPU control through serial I/F
13) QFN28V package (5.2mm × 5.2mm)

*This chip is not designed to protect itself against radioactive rays.

@Absolute Maximum Ratings

(unless otherwise noted, Ta = 25°C)

Parameter	Symbol	Rating	Unit	Remarks
Power supply voltage	VDD	-0.3 - +4.5	V	
Voltage applied to pin	VIN	DVSS-0.3 - DVDD+0.3	V	
Input current	IIN	-1 - +1	mA	
Allowable dissipation	Pd	370*1	mW	The guaranteed value for the single unit IC
Storage temperature range	Tstg	-50 - 125	°C	
Operating temperature range	Topr	-40 - 85	°C	

*1 When Ta is above 25°C, reduce 3.7mW per 1°C.

@Recommended operating conditions

(unless otherwise noted, Ta = 25°C)

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage	VDD	2.7	3.0	3.6	V	
Ambient temperature	Ta	-40	25	85	°C	
MCLK input frequency	FMCLK	12.5	-	18	MHz	Scale precision is within 0.2%
SCLK input frequency	FSCLK	-	-	MCLK	MHz	
MCLK duty	DMCLK	40	50	60	%	
SCLK duty	DSCLK	40	50	60	%	
ANOUT pin load resistance	ZAN	12	-	-	kΩ	The AC load resistance value. Apply to ANOUT-R,ANOUT-L and ANOUT-Mono pins.

@Block Diagram

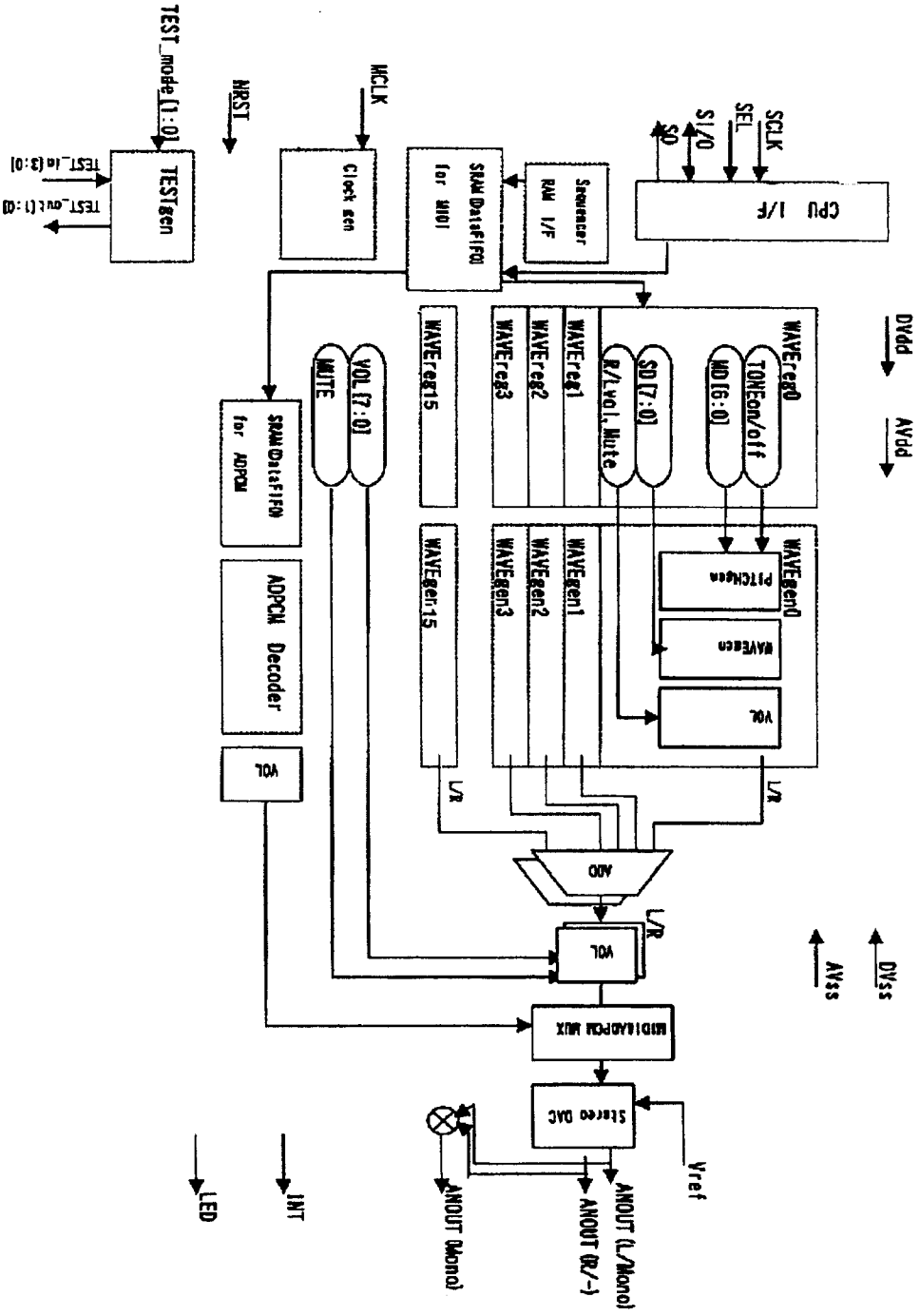


Fig.1 Block diagram

Description of the circuit blocks

@ Serial interface block

This is an interface circuit with the system LSI.

In write mode, it receives serial data synchronized with SCLK pin at the SI/O pin, converts them to parallel data, and passes them to the WAVEreg or SRAM block.

In read mode, it converts data from WAVEreg to serial data, and outputs them synchronized with SCLK at the SI/O and SO pin.

@ Sequencer block

This is a block to analyze and convert the message data.

When playing a melody, it analyzes the RAM read data to perform the settings required for the melody at the desired timing in the WAVEreg block.

It has dynamic assigning function to each WAVEgen.

@ RAM Interface block

This block controls the SRAM. It generates and controls the write and read pointers to configure FIFO buffer for music data.

@ SRAM (FIFO)

This is a buffer used for the sound source and ADPCM data. It constitutes FIFO.

The memory size is 512 bytes for the sound source and 256 bytes for ADPCM.

The write point (WP) and read point (RP) are controlled with the hardware. NearlyEmpty and NearlyFull interrupts are provided to prevent overflow and underflow errors.

Both WP and RP are reset and FIFO memories are emptied by setting SequenceControlReg Reset bit to "1".

@ Timing gen block

This block controls timing to play music. It controls timing to access the WAVEreg block.

@ Clock gen block

This is a clock generator to supply clocks to the Sequencer and WAVEgen block.

The master clock supplied from MCLK pin generate division parameters to maintain a constant output frequency from each WAVEgen block's internal divider/counter to enable to support system clocks for sequencer and WAVEgen block for various master clocks (MCLK).

@ WAVE register

These are the control registers of the block to generate sounds.

The Sequencer controls the WAVEgen block.

The control register of the WAVEgen block can also be accessed directly by the CPU.

Common control of the sound sources is controlled directly by the CPU.

@ WAVEgen block

This is a block to generate sound (melody) wave forms. Up to 16 sounds can be generated at the same time.
It generates waveforms according to the data set in the WAVEreg register.
There are 16 sound sources to generate 128 tones, drum set and specific effect sounds.
As for scale, sounds can be generated within recommended sound area of each tone shown in p30.

@ ADPCM block

This is a ADPCM decoder block. It can generates user's own sounds.
It supports 8K Fs or 4K Fs sampling rate to allow mixing with MIDI.
It stops when the FIFO is emptied.

@ DAC

This is a stereo D/A converter.
The analog output level is decided by adding sound levels of up to 16 WAVEgen registers and also sound level of the ADPCM. As the dynamic range of DAC block is 2/3 Vdd in Vpp, be careful that the amplitude of the synchronized sound from 16 sound sources and ADPCM is within this range. Outside of the dynamic range, sounds can have distortion to cause unnatural sense of hearing.
Amplitude control is performed with the register MIDI WaveVol (address 0x01) and ADPCM WaveVol (address:0x02).
Set a value in the register not to cause unnatural sense of hearing for each music.

@ LPF

This is a secondary LPF (Low Pass Filter).
It is a smoothing filter to eliminate high frequency components from the analog waveforms generated in the DAC block.
The final analog waveforms are output via ANOUT pin.
The minimum load resistance to be connected to ANOUT pin is 12 [kΩ].

@ Interrupt Control

It controls the interrupt sources of ADPCM, the sound source FIFO, Timer, LED, Call back and so on.
Active when one of bit2, 1 or 0 of the register INT Status (address:0x03) is "1".

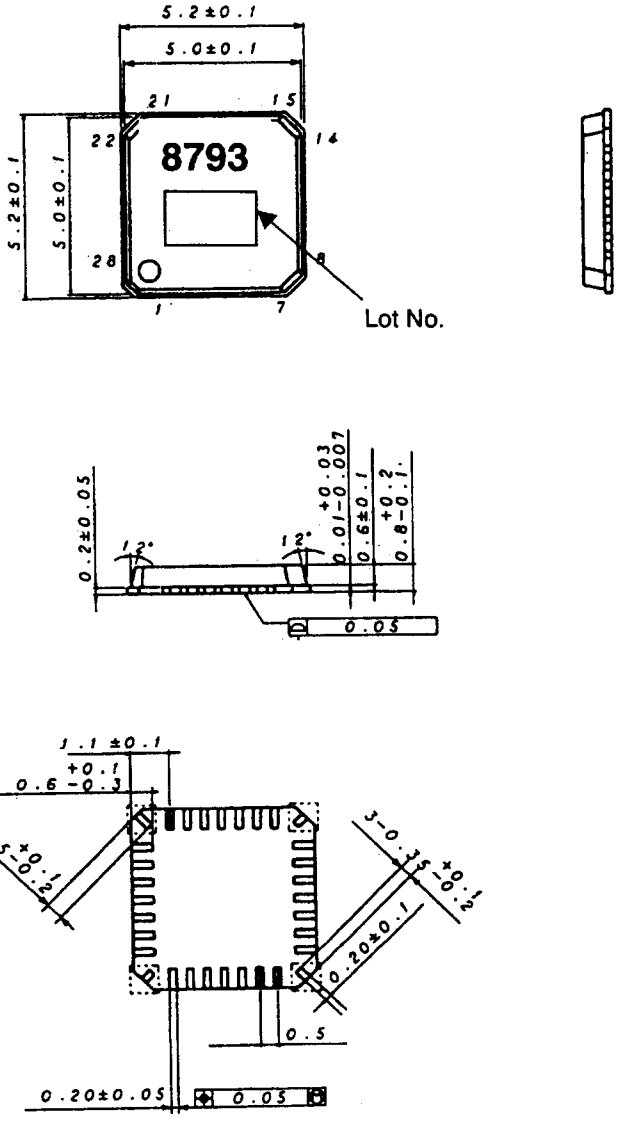
@ LED Control

This is a LED signal generator
It can be turned on by synchronizing with a music data specified to be the main melody (Track 0, Voice0), or by the register directly. It is turned off with the register.
For details, see LED control in p35.

@ Test block

This is a LSI testing circuit.
When TEST_mode [1:0] pins are set to "H,H"(DVdd), the LSI is in normal mode.
In other cases, the LSI is in test mode.
Usually, set Test_in pin [3:0] to DVdd, and Test_out pin [1:0] to NC.

@Mechanical dimension



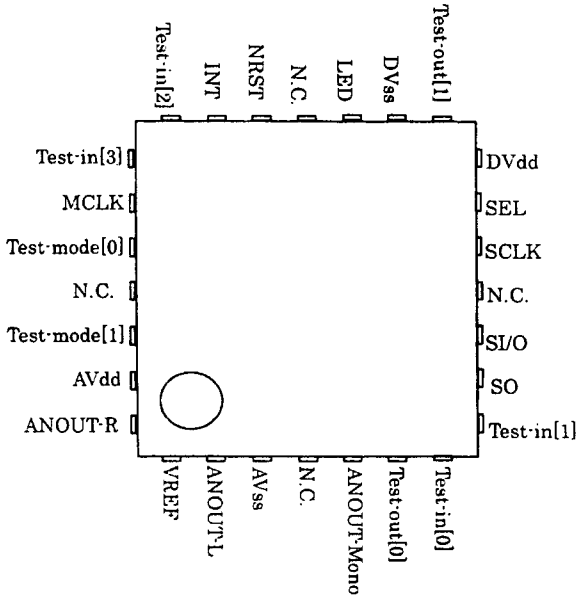
注）点線部は実装を推奨しておりません

NOTICE) Not recommend soldering the part of the dotted line.

(Unit: mm)

Fig.1 QFN28V Mechanical dimension (plastic mold)

@Terminal Assignment

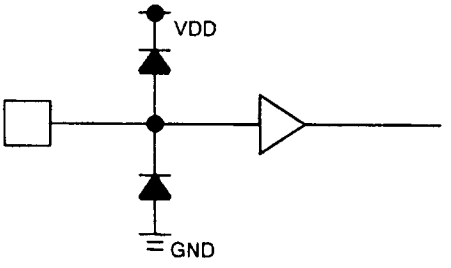
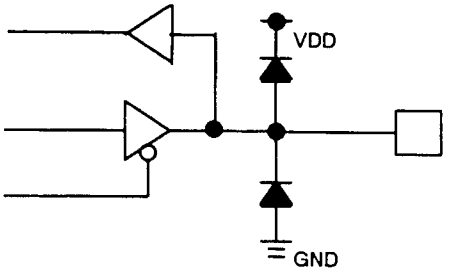
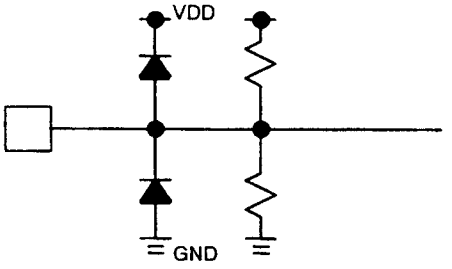
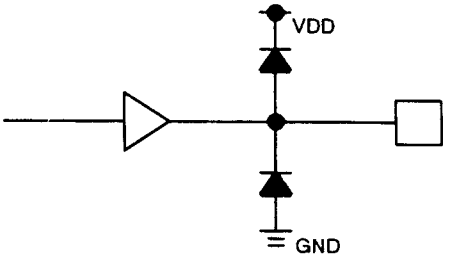
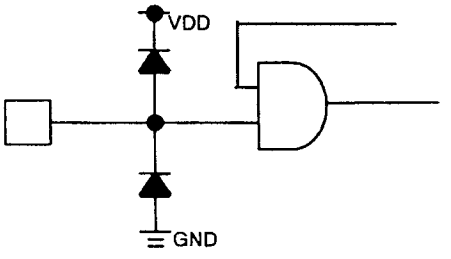
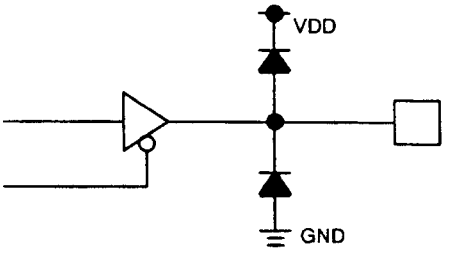
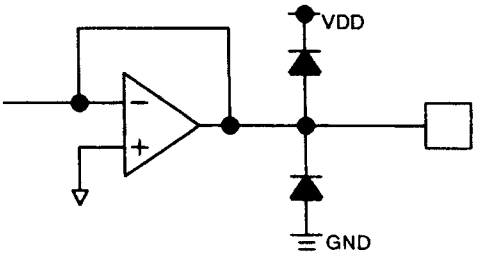


@Description of pin functions

Pin No.	Symbol	Description of function	Attribute	Circuit type	Remarks
15,6	Test-out[1:0]	Output pin for LSI test.	Out	F	Open during operation
20	INT	Interrupt pin of this IC. "L" for active ("H" for active can also be set.) Active when one of bit2, 1 or 0 of address 0x03 is "1".	Out	D	
17	LED	Output pin for LED light timing	Out	D	
14	DVdd	Digital power supply pin	-	-	
16	DVss	Digital ground pin	-	-	
22,21 8,7	Test-in[3:0]	Input pin to set LSI test Connect it to DVdd pin.	In	A	Connect to DVdd during operation
28	ANOUT-R (R)	Analog output pin. The potential of this pin is approximately same as Vref when not playing. It is equal to Hi-z when it is reset, and to Vref when it is set to monophonic mode.	Ana	G	
1	VREF	AC (signal) ground pin Connect a 1μF by-pass capacitor between Vref and ground pin. When you use the differencial output between ANOUT-L and ANOUT-Mono, we suggest that VREF pin open, take by-pass capaciter off, because it decrease noise from AVDD line.	Ana	C	
2	ANOUT-L (L/Mono)	Analog output pin. The potential of this pin is approximately the same as Vref when not playing. It is equal to Hi-z when it is reset. This pin outputs monophonic output when it is set to monophonic mode.	Ana	G	
3	AVss	Analog ground pin	-	-	
27	AVdd	Analog power supply pin	-	-	
5	ANOUT-Mono (Mono)	Analog output pin. The potential of this pin is approximately the same as Vref when not playing. It is equal to Hi-z when it is reset. This pin outputs monophonic sound. When set to monophonic mode, inverted signal of ANOUT-L terminal (Mono) is output.	Ana	G	
26,24	Test-mode[1:0]	Input pin to set LSI test Connect it to DVdd pin.	In	A	Connect to DVdd during operation
23	MCLK	System clock input pin Any frequency can be selected between 12.5MHz and 18MHz. The scale precision within this range is approximately 0.2%.	In	E	
9	SO	Data output pin for serial interface. When SEL input is "H", the potential of this pin is equal to Hi-z.	Out	F	
10	SI/O	Data input/output pin for serial interface.	In/Out	B	
12	SCLK	Clock input pin for serial interface	In	A	
13	SEL	Select input pin for serial interface. Set to "L" to activate.	In	A	
19	NRST	Reset input pin. Set to "L" to activate.	In	A	

* Use the chip with the same voltage of DVDD (digital power supply) and AVDD (analog power supply).

@I/O circuit diagram

Input circuits		Output circuits	
A		B	
C		D	
E		F	
		G	

@Electrical Characteristics (1)

(unless otherwise noted, Ta = 25°C)

Parameter	Symbol	Rating Min.	Rating Typ.	Rating Max.	Unit	Remarks
Digital DC characteristics						
High-level input voltage	VIH	0.7DVDD	-	-	V	
Low-level input voltage	VIL	-	-	0.25DVDD	V	
High-level input current	IIH			10	μA	VIH=DVDD
Low-level input current	IIL	-10	-	-	μA	VIL=DVSS
High-level output voltage	VOH	DVDD-0.3	-	-	V	IOH=-0.8mA
Low-level output voltage	VOL	-	-	DVSS+0.3	V	IOL=0.8mA
Analog DC characteristics						
VREF pin voltage	VAGND	0.475AVDD	0.5AVDD	0.525AVDD	V	IOUT=0A (no load)
ANOUT pin voltage	VOUT	0.47AVDD	0.5AVDD	0.53AVDD	V	IOUT=0A (no load) when not playing
General characteristics						
VREF pin rise time	TRVR	-	70	100	mS	When Capa=1μF between VREF and AVss NRST=L→H
Analog (ANOUT pin) characteristics						
ANOUT amplitude	VMAX	-	0.667 AVDD	-	Vp-p	Theoretical value of dynamic range

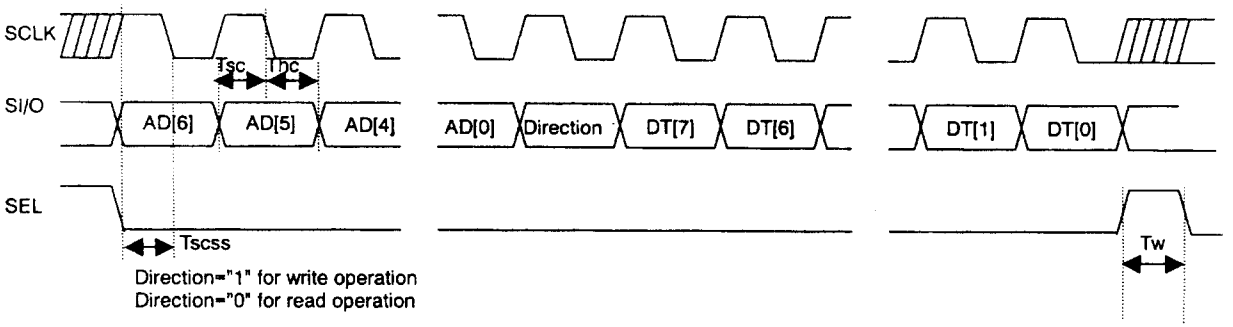
Current consumption	Vdd=3V, Internal operation frequency=13MHz					
Analog Idd	IDD1	-	1.3	3	mA	Playing
Digital Idd	IDD2	-	16.5	22	mA	Playing
Analog Idd	IDD3	-	-	1	μA	Standby mode
Digital Idd	IDD4	-	-	1	μA	Standby mode

@Electrical Characteristics (2)

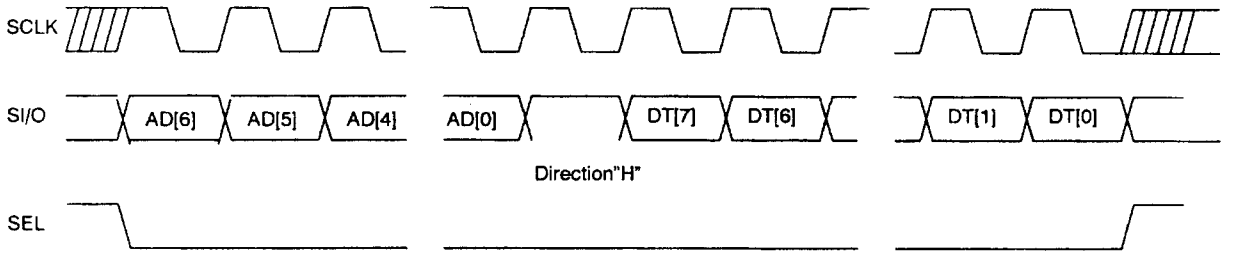
(unless otherwise noted, Ta = 25°C)

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Serial interface format						
Character bit length	Ncha	16	-	-	bit	MSB first
Serial interface characteristics						
SCLK input frequency	FSCLK	-	-	MCLK	MHz	
SCLK duty	DSCLK	40	50	60	%	
SEL "H" pulse width	Tw	25	-	-	nS	
SCLK-SEL setup time	Tscss	25	-	-	nS	to falling edge of SCLK
Data setup time	Tsc	25	-	-	nS	to falling edge of SCLK
Data hold time	Thc	25	-	-	nS	to falling edge of SCLK

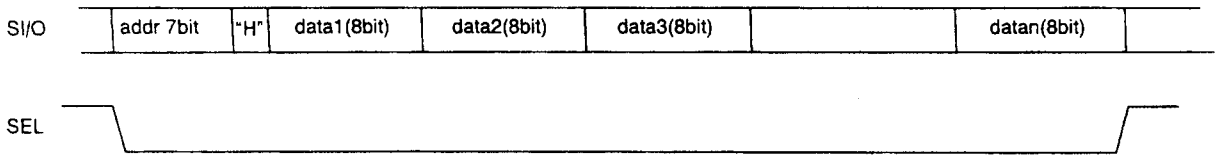
Serial interface timing chart



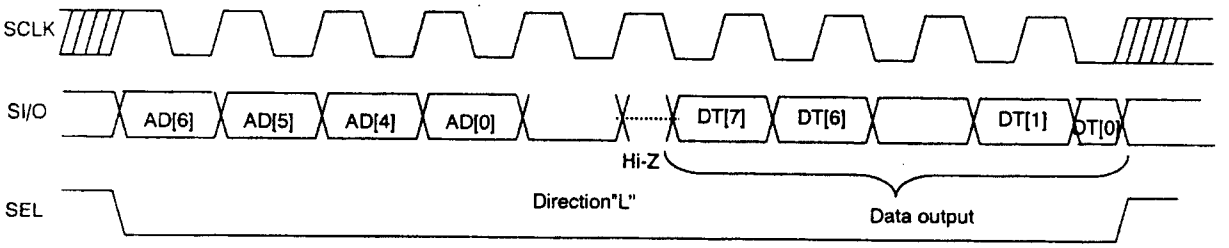
Write operation



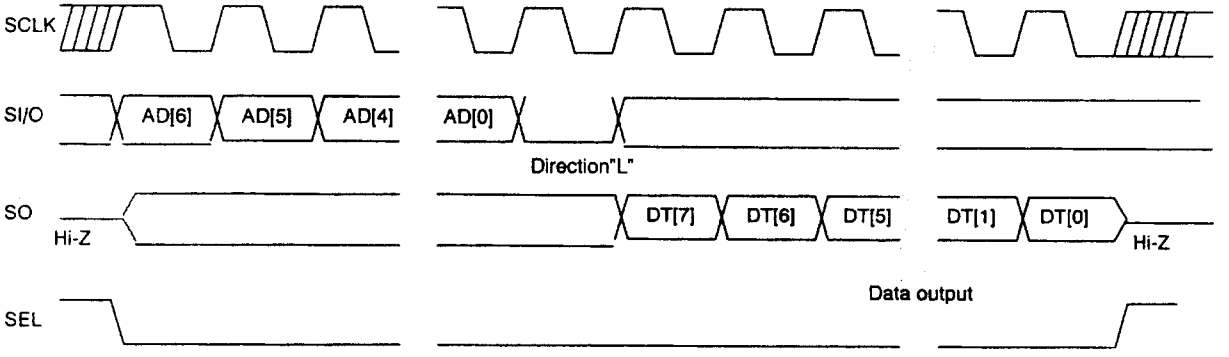
While SEL is held to "L", data (in 1 byte) can be written successively into a same address.



Read operation (SI/O output): Output is synchronized to a falling edge of SCLK.
Output only when bit3 of address 0x00, Pmode = 0.



Read operation (SO output): Output is synchronized to a rising edge of SCLK.

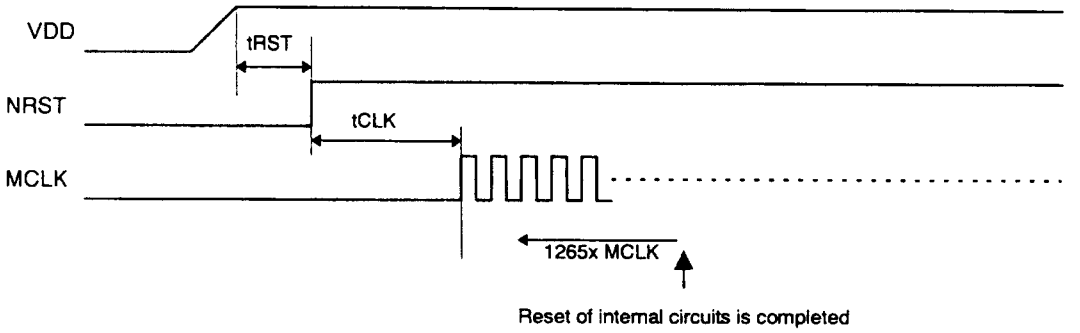


@Electrical Characteristics (3)

(unless otherwise noted, Ta = 25°C)

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Reset sequence						
VDD→NRST time	TRST	10	-	-	ms	
NRST→MCLK time	TCLK	0	-	-	ms	MCLK waveform must be normal.

<Pin reset sequence>



* Be sure to reset the system after the power is turned on.
* This sequence represents the external terminal, NRST.
  This does not corresponds to the soft-reset (bit7 of register address 0x07).

CPU interface

This IC has CPU interface of serial .

The interface signal is composed of 7-bit address, 1-bit direction, and 8-bit in/out data.

Write operation: The address, direction and data are fixed at the negative edge of SCLK.

Read operation: The address and direction are fixed at the negative edge of SCLK. The data are output from SO at the positive edge, and from SI/O at the negative edge. (Selected with bit 3 of address 0x00).

Description of the sequencer

This sequencer controls the timing of the sound sources according to the timing information in the melody data.
To take full advantage of the sound sources, it also has dynamic data assigning function to the sound sources.
These function allows high quality musical expressions.

[Outline of operation]

1) It fetches melody data stored in FIFO registers and assigns them to empty sound sources.
2) It sets the melody data into a WAVEgen Setup register to generate a tone.
3) It controls tone generation timing and turn the tone off at the tone end timing to release the sound sources.
4) It decides priority to assign the sound source according to the Track Number and the Voice Number.
   If melody data with more than 16 tones are fetched, one of the tones played currently is deleted forcedly and a new tone is played. The tone to be deleted is decided according to Track Number and Voice Number. Since a tone with a lower Track Number and Voice Number has higher priority, assign a low Track Number or Voice Number to the important tones, such as main melody or drum set.
   The algorithm to decide a tone to be deleted is as follows:
   ① A tone with highest Track Number is selected. If multiple tones are found,
   ② Among tones selected in step ①, a tone with highest Voice Number is selected. If multiple tones are found,
   ③ Among tones selected in step ②, a tone to which highest WAVEgen Number is assigned is selected.

The following shows the control data in the WAVEgen block.
This data is stored in the LSI and controlled by the Sequencer.
It can be accessed from the CPU via the Wave Window register.

SD[7:0]	Tone data
MD[6:0]	Scale data
PitchBend[9:0]	PitchBend sensibility (PitchBend[9]:±directive bit)
LV[5:0]	Left channel volume data
RV[5:0]	Right channel volume data
Vib[6:0]	Vibrato parameter