



Atheros AR8032 10/100M Ethernet Transceiver

Design Guide

Rev. 1.2

Atheros Communication Inc.



ATHEROS®

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1. Introduction

AR8032 is a single port 10BASE-T and 100BASE-TX Ethernet PHY transceiver and performs physical layer functions on CAT5 unshielded twisted pair cable. AR8032 supports MII/RMII (Reduced MII) interface for MAC and can be configured through CONFIG[2:0] strapping. AR8032 has a small package 32-pin QFN (5 x 5 mm) with an exposed ground pad, makes AR8032 the ideal choice for 10/100M LAN PHY.

AR8032 includes two versions, commercial version and industry version. There is only power design difference between two versions of AR8032. The power design difference has been specified in section 9.

1.1 Features

- 10/100 BASE-T IEEE 802.3 compliant
- Supports MII/RMII interface
- Low power modes with internal automatic DSP power saving scheme
- Fully integrated digital adaptive equalizers All digital baseline wander correction
- Supports external 25 MHz clock source for XI (1.5V level) or 25MHz crystal for XI/XO.
- Supports a 50 MHz shared-source clock in RMII mode.
- Automatic speed downshift mode
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- Loopback modes for diagnostics
- IEEE 802.3u compliant Auto-Negotiation
- Software programmable LED modes
- Cable Diagnostic Test (CDT)
- Requires only one 3.3V power supply
- 32-pin QFN 5 mm x 5 mm package

1.2 Functional Block Diagram

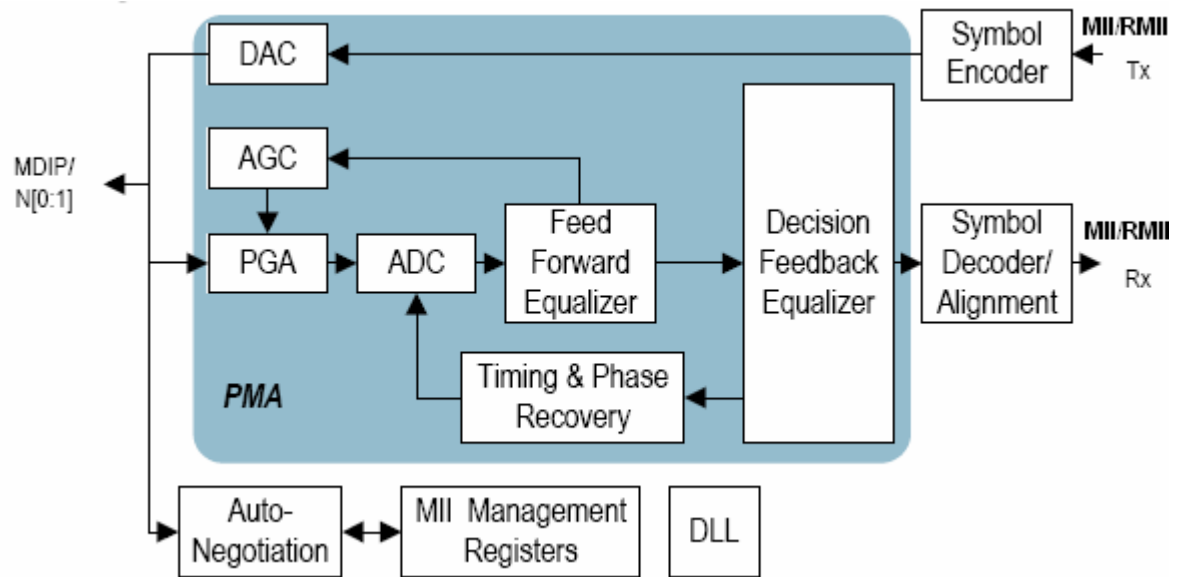


Figure 1: Functional Block Diagram

1. 1 Guidelines

This design guide is composed of chip interfaces, power and ground, system signals design and layout guide, power on strapping function, industry version chip design guide.

3. Pin out

The following diagram *Figure 2* shows the pin-out and descriptive names given to each pin, as viewed from the top of the chip package. For more detailed pin descriptions and functions, refer to the AR8032 datasheets.

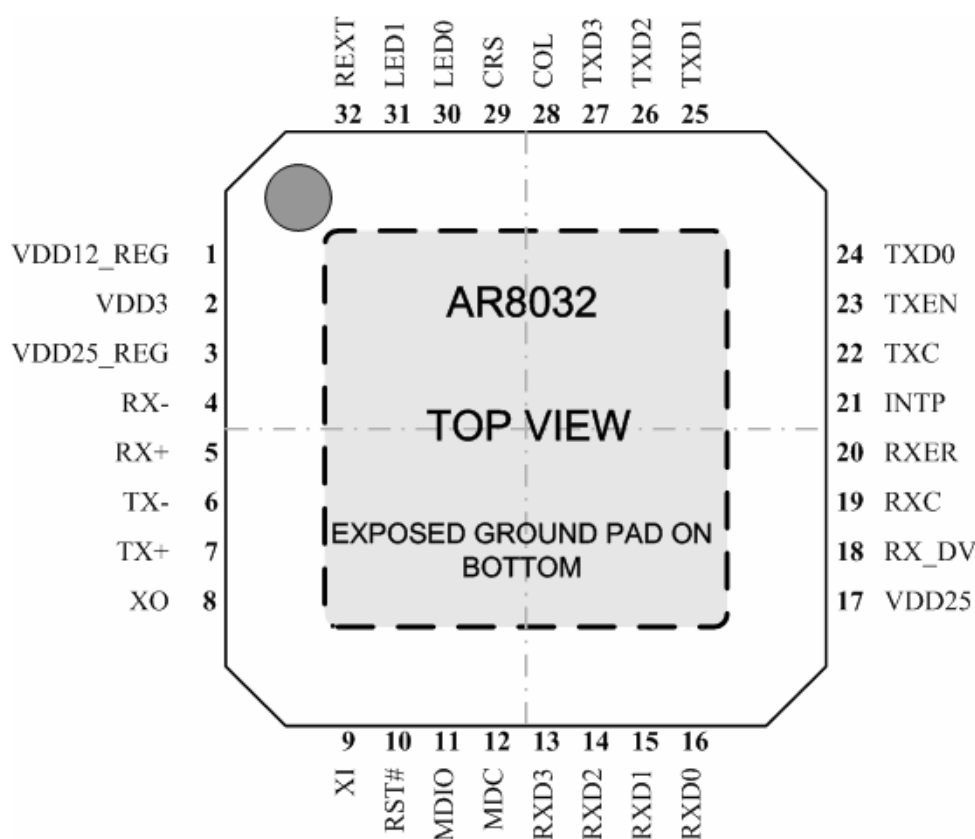


Figure 2: Pinout Diagrams-Top View

Note: There is an exposed ground pad on the back side of the package.

There are 4 groups of pins. The first group forms interfaces, such as MDI, MII/RMII and LEDs. The second group consists of special system signals such as clock, reset, REXT pin. The third group consists of power and ground pins. The fourth group is made up of power-on strapping pins which are multiplexed with some interface pins.

4. MDI Interface

Table 1 shows the pin map and pin description of the MDI interface.

Table 1: MDI interface pin map and description

Symbol	Pin	Type	Description
RX-	4	IA,OA	Media Dependent Interface 0, terminate with a 49.9Ω resistor and connect to XFMR
RX+	5	IA,OA	Media Dependent Interface 0, terminate with a 49.9Ω resistor and connect to XFMR
TX-	6	IA,OA	Media Dependent Interface 1, terminate with a 49.9Ω resistor and connect to XFMR
TX+	7	IA,OA	Media Dependent Interface 1, terminate with a 49.9Ω resistor and connect to XFMR

The schematic circuit of MDI interface is shown as Figure 3.

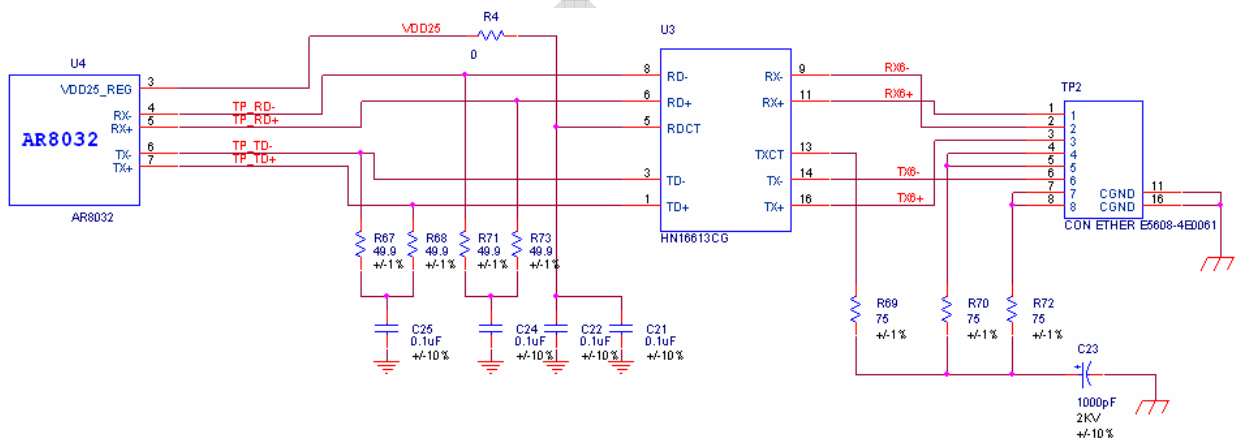


Figure 3: MDI Interface Schematic Circuit

On the AR8032 chip side of schematic circuit, two pairs of differential traces connect to MDI interface directly with $49.9\Omega \pm 1\%$ termination resistor and $0.1\mu\text{F}$ capacitor decoupling. They are kept as close to the pins as possible. Transformer ratio is 1:1 and center taps need 2.5V power source as DC reference voltage.

On the RJ45 jack side of the circuit, two pairs of differential traces connect to RJ45 pins and 75Ω termination resistors connect to the center tap. This termination is named as Bob Smith termination. A “Bob Smith” termination is often provided for the media-side center-taps. This circuit is used to enhance EMI and ESD

performance of the system. The Bob Smith termination can provide termination for the media-side center-taps and is comprised of individual 0.001uF, 2kV capacitors to chassis ground. Separate capacitors are used for the receiver and transmitter center-taps. This improves isolation by eliminating the low impedance path between receiver and transmitter that would exist if a single common capacitor was used. The capacitors provide a high-frequency path to ground, enhancing ESD and EMI performance. For detail information of Bob Smith termination you can refer to US patent US005321372.

AR8032 supports channel 0 and 1 of MDI automatically crossover function and polarity automatically correct function. We can layout the two pairs of differential trace favoringly and conveniently through swapping channel 0 and channel 1 or swapping polarity within channel based on the two functions.

The MDI PCB layout rules are illustrated in *Figure 4*.

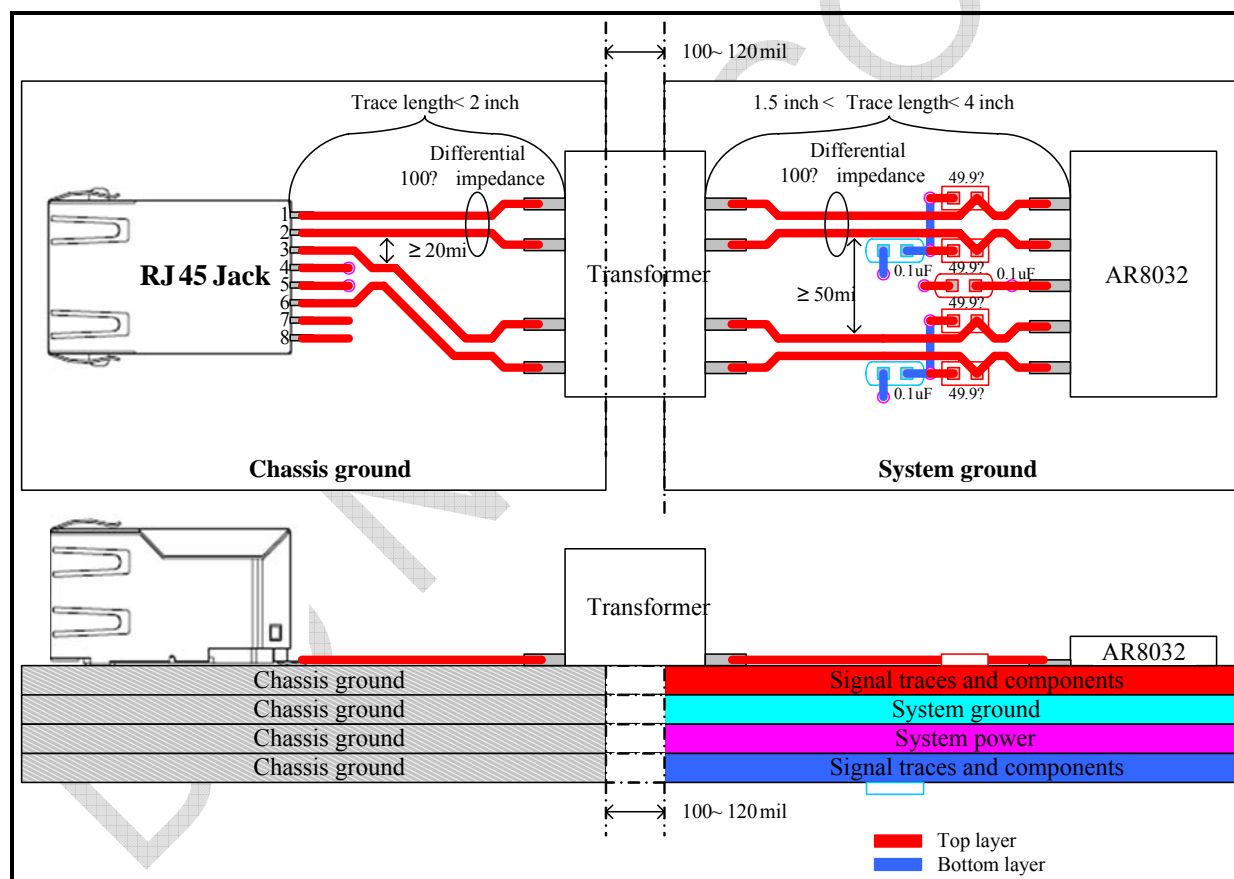


Figure 4: MDI Interface Trace PCB Layout

Two pairs of differential traces between transformer and RJ45 should be laid out as 100Ω differential impedance and equal length as possible (maximum tolerance 25mils). The length between RJ45 and transformer should be

less than 2inch. To minimize cross talk, the space between separate adjacent pairs that are on the same layer should be 20mils or more. This minimizes signal skew and common mode noise and improves long cable performance.

Two pairs of differential traces between AR8032 and transformer should be laid out as 100Ω differential impedance and equal length as possible (maximum tolerance 10mils). The length between AR8032 and transformer should be at least 1inch and less than 4inch. Signal attenuation will cause problems for trace longer than 4inch. AR8032 should be placed at least 1inch away from transformer for EMI. To minimize cross talk, the space between separate adjacent pairs that are on the same layer should be 50mils or more. In the clearance area, ground should be placed fill along the differential pairs.

The split in ground plane should be at least 100~120mils. The split should run under center of transformer. Differential pairs never cross the split. Clearance constraint between 4 differential pair trace and chassis ground is 70~75mils. Keeping this clearance can improve EMI behavior. If PCB is four layers, all layers design should abide by the same layout rule.

Two pairs of differential trace width should be designed to handle the amount of current that are expected. If PCB material is FR4 epoxy glass cloth laminated sheets and its relative dielectric constant is $\epsilon_r=4.3$, the recommended differential trace width is 8mils and the gap is 7mils.

Transformer Selection

It is a key point to select transformer for AR8032. Good EMI control can be gotten especially on low frequency bandwidth (30M~100MHz) if 8 core transformer with common choke on chip side is selected. The performance of 8 core transformer with 3 lines common chokes is better. The performance of 12 core transformer is the best but the price is expensive.

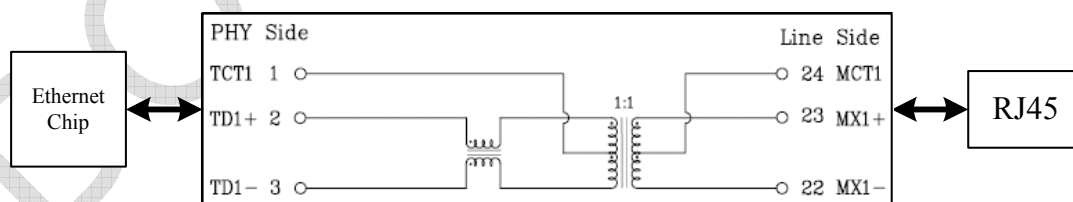


Figure 5: Transformer with 8 cores and 2 lines common choke on chip side

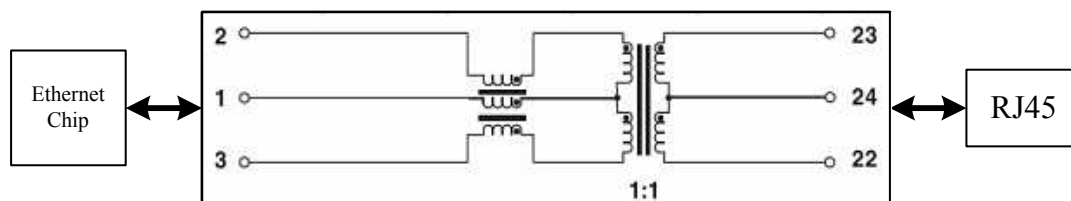


Figure 6: Transformer with 8 cores and 3 lines common choke on chip side

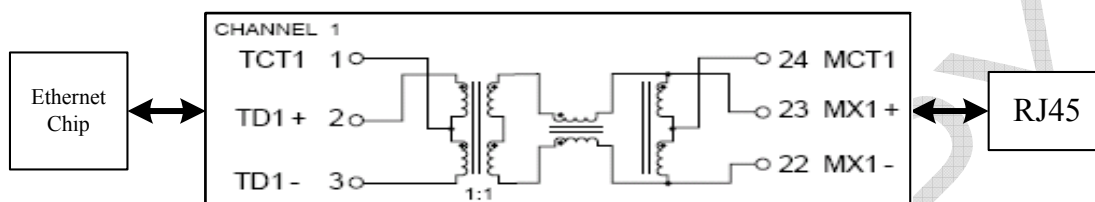


Figure 7: Transformer with 12 cores

5. MII/RMII Interface

Table 2 shows the pin map and pin description of the MII/RMII interface.

Table 2: MII/RMII interface pin map and description

Symbol	Pin	Type	Description
RXC	19	I/O,PD POS	MII receive clock output, 25MHz digital, adding a 22Ω damping resistor is recommended
RX_DV	18	I/O,PD POS	MII receive data valid / RMII Carrier Sense & receive data valid output, adding a 22Ω damping resistor is recommended.
RXD0	16	I/O,PU POS	MII/RMII Receive data output [0], adding a 22Ω damping resistor is recommended
RXD1	15	I/O,PD POS	MII/RMII Receive data output [1], adding a 22Ω damping resistor is recommended
RXD2	14	I/O,PD POS	MII Receive data output [2], adding a 22Ω damping resistor is recommended
RXD3	13	I/O,PU POS	MII Receive data output [3], adding a 22Ω damping resistor is recommended
RXER	20	I/O,PD, POS	MII Receive error output
TXC	22	I/O,PU, POS	MII transmit clock output, 25MHz digital, adding a 22Ω damping resistor is recommended
TXEN	23	I,PU	MII/RMII transmit enable
TXD0	24	I,PD	MII/RMII transmit data input [0]
TXD1	25	I,PD	MII/RMII transmit data input [1]
TXD2	26	I,PD	MII transmit data input [2]
TXD3	27	I,PD	MII transmit data input [3]
COL	28	I/O,PD POS	MII Collision Detect output
CRS	29	I/O,PD POS	MII Carrier Sense output
MDC	12	I,PU	Management data clock reference
MDIO	11	I/O,D,PU	Management data, 1.5kΩ pull-up resistor to 3.3V

The schematic circuit of MII interface is shown as *Figure 8*.

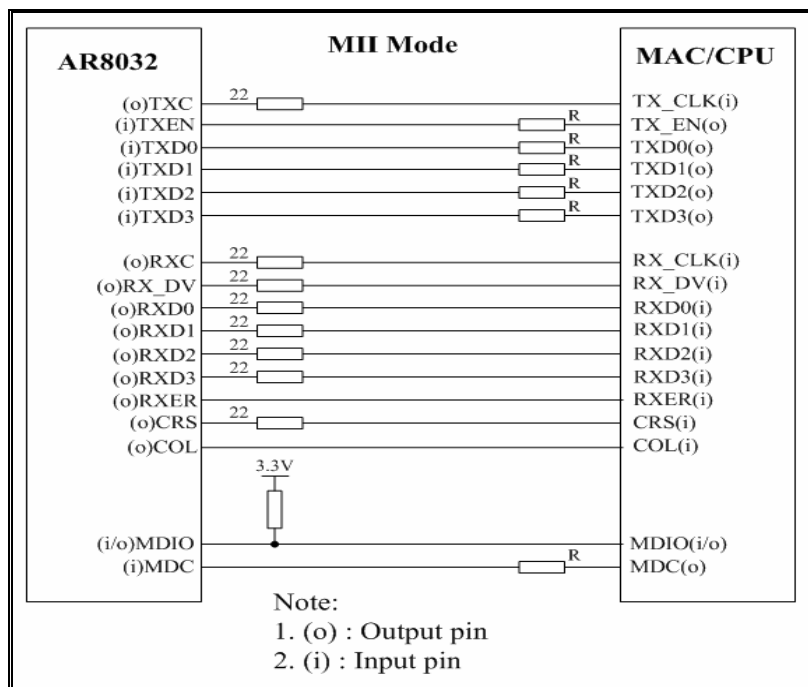


Figure 8: MII interface

AR8032 data transmission relies on MII/RMII interface with MAC. It is parallel to clock signal which clock frequency is 25/50MHz. Care must be taken on data bus and clock compatibility during layout to avoid signal cross talk so as to effecting clock and data bus signal's performance and making receiving data error. TXEN and TXD[0:3] are in series with damping resistor R which value between 0Ω and 49.9Ω . In addition, TXC, RXC, RX_DV and RXD[0:3] are in series with 22Ω dumping resistance and hardware configure resistance ($10k\Omega$ pull high or pull low for power on strapping), see Section 8 Power On Strapping.

For RMII mode, AR8032 needs a 50MHz REFCLK for RMII. This clock should be injected in to XI pin on AR8032 from an external clock source, either from CPU/MAC side or an external oscillator. It is noted that the REFCLK injected into XI pin should has about 1.2V swing, less than 1.5V, meanwhile the XO pin should keep floating. Usually the typical clock swing from CPU/MAC side or an external oscillator is 3.3V, in order to fit AR8032 requirement, we can use resistors or one capacitor to meet the requirement.

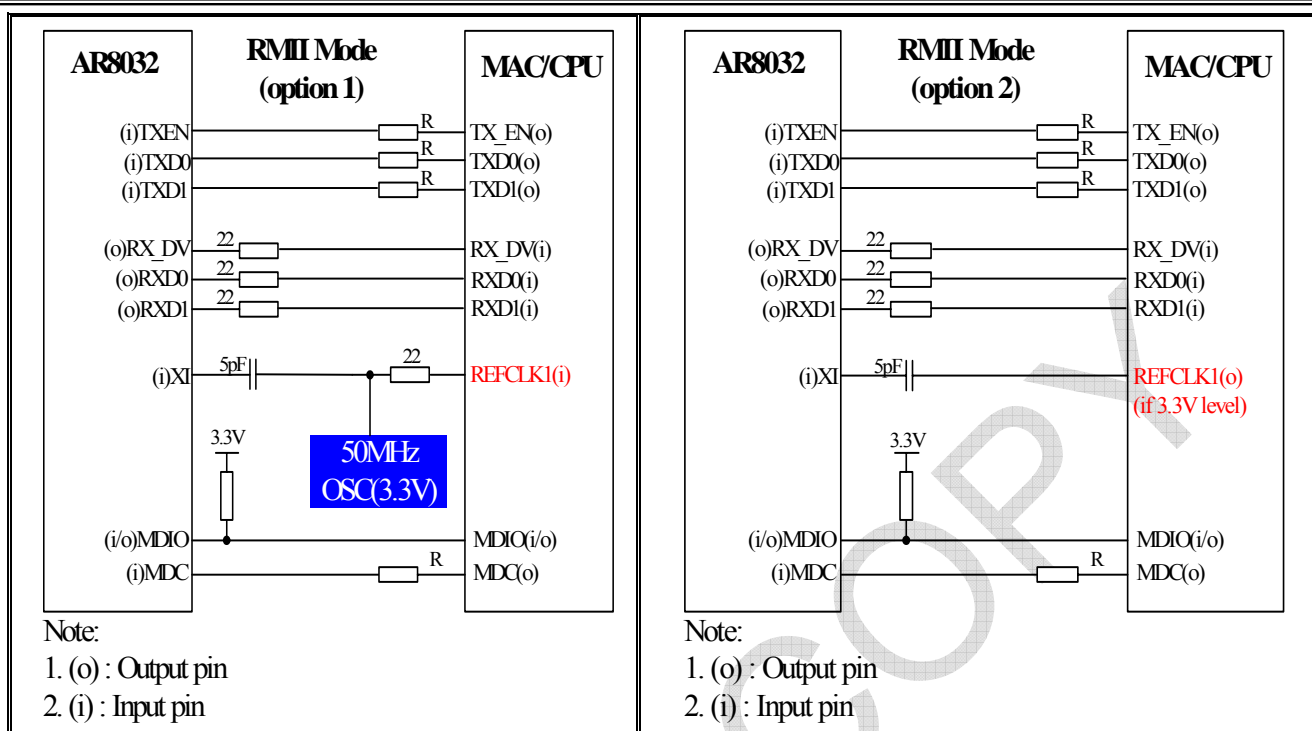


Figure 9: RMII interface (Option 1&2)

When using capacitor, Figure 9 shows the schematic for RMII interface. When layout, the 5pF capacitor should be placed closed to XI pin on AR8032. Option 1 shows REFCLK is from an external oscillator and option 2 shows REFCLK is from CPU/MAC side.

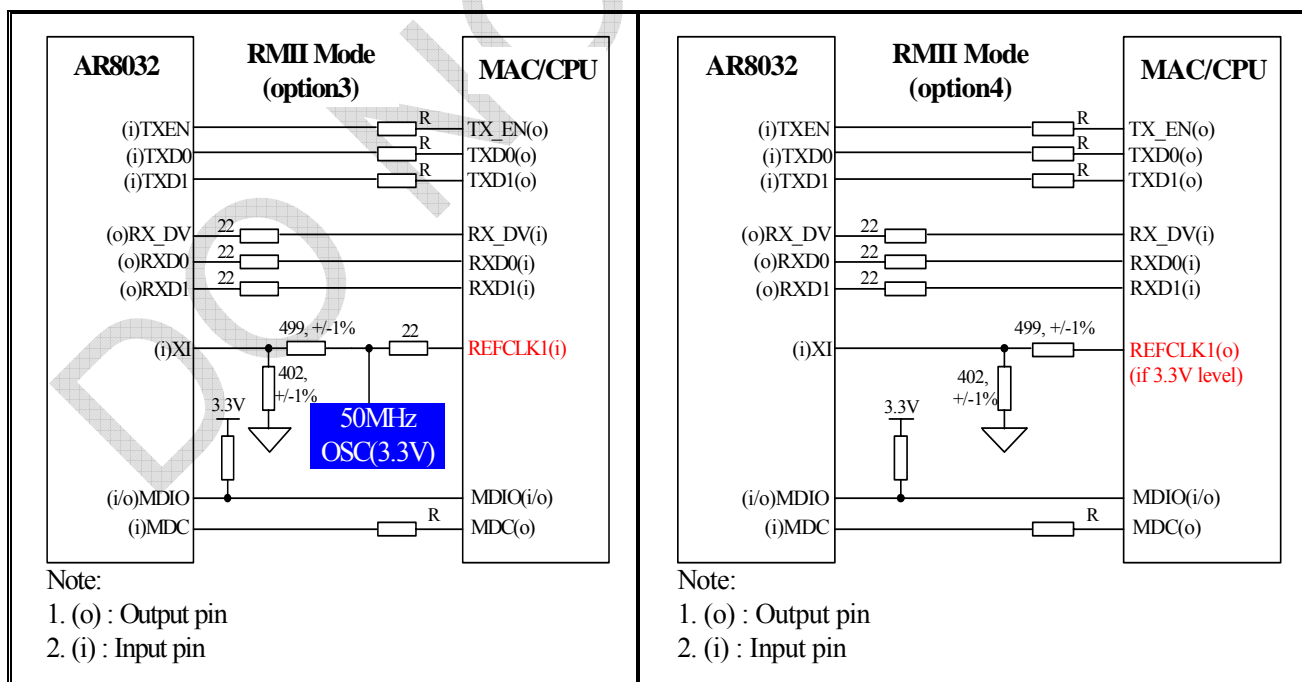


Figure 10: RMII interface (Option 1&2)

When using resistors, *Figure 10* shows the schematic for RMII interface. Option 3 shows REFCLK is from an external oscillator and option 4 shows REFCLK is from CPU/MAC side.

Some PCB layout rules should be used in PCB design. Equal trace length (maximum tolerance 100mils) and 45 degree or arc layout cornering are recommended. Do not route trace with 90 degree turns. *Figure 11* shows the trace routing rule.

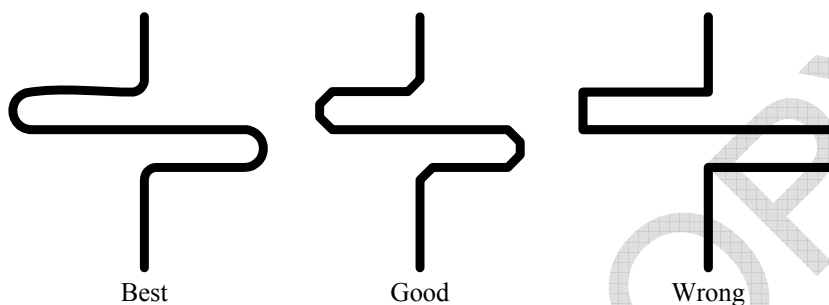


Figure 11: Trace routing rule

Maximum trace length of MII/RMII interface is 15 inch, $50\Omega \pm 10\%$ single end impedance and at least 12mils space for each trace is need. All MII/RMII traces should be referenced to an uncut ground or power plane. Especially for RXC and TXC traces, they are two sensitive and critical signals. It is very important that the two signal routing traces must be separated from other data bus and routed along with ground trace both sides or relies on ground fill area. Sometimes in high density layout design such as little size motherboard, the two traces route on different plane through vias for far away from neighboring signal (more than 20mils) to cut down crosstalk. *Figure 12* shows one example for all trace on same layer.

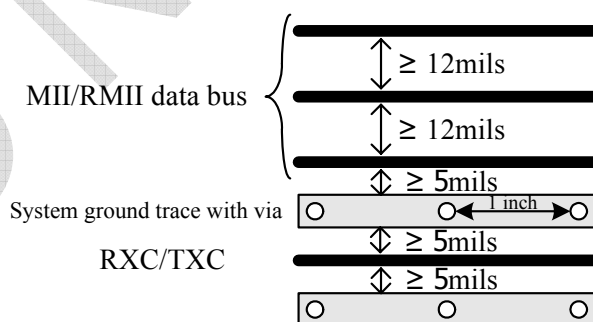


Figure 12: Trace routing rule for MII/RMII interface

Because input pins on MII/RMII interface such as TXC, RXC, RX_DV, RXER and RXD[0:3] are also multiplexed as power on strapping, it is important to layout power on strapping resistors. For more information about power on strapping, please refer to Section 9 Power On Strapping. The layout rules of these signals are

illustrated as shown in *Figure 13*, using RXD1 as example.

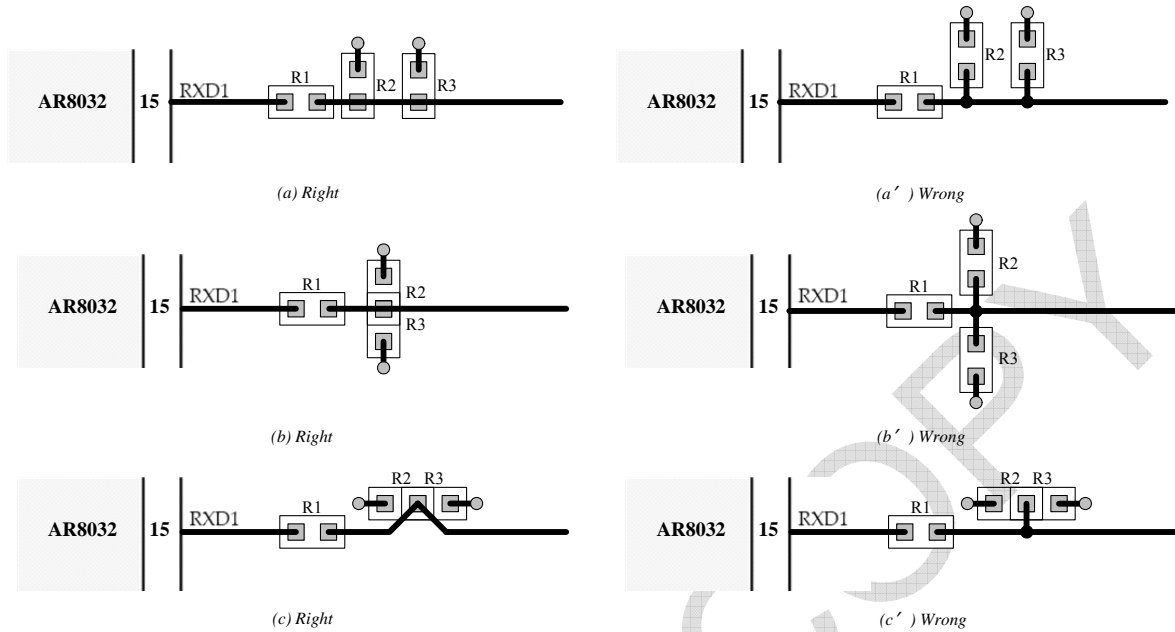


Figure 13: Input MII/RMII trace routing with pull high or pull down resistor

On the left side, *Figure 13(a)*, *(b)* and *(c)* show the right layout rule for 22Ω dumping resistor and pull high/low resistor with three examples. At the same time, on the right side, *Figure 13(a')*, *(b')* and *(c')* show the wrong layout routing versus left side ones. The basic rule is to keep one main trace without any bifurcate and short ones.

6. LED interface

The LED interface includes two LED pins. Table 3 shows the pin map and pin description of the LED interface.

Table 3: LED interface pin map and description

Symbol	Pin	Type	Description
LED0	30	I/O, PU POS	Programmable LED0. The LED0 default function is for 10/100M link and activity. When recommend value during power on is high, then this signal is active low; if the recommend value is low, then this signal is active high. <ul style="list-style-type: none"> 1. LED off: No Link. 2. LED on: Link-up. 3. Blinking: Transmit or receive activity
LED1	31	I/O, PU POS	Programmable LED1. The LED1 default function is for 10/100 M speed. When recommend value during power on is high, then this signal is active low; if the recommend value is low, then this signal is active high. <ul style="list-style-type: none"> 1. LED off: No Link or 10M. 2. LED on: 100M.

The schematic circuit of LED interface is shown as Figure 14.

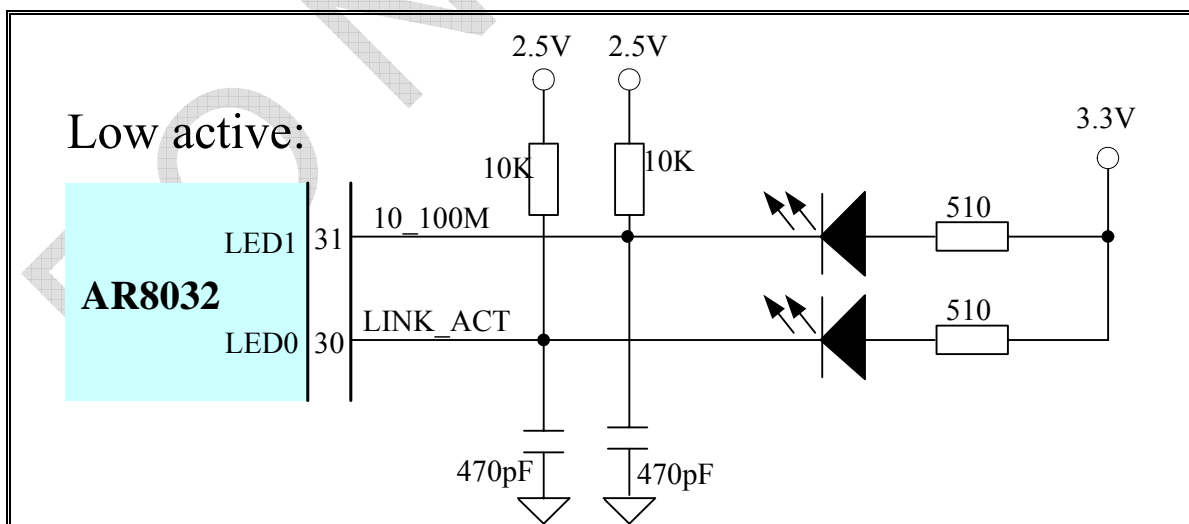


Figure 14: two special LED circuit with pull up resistor

One LED pin should drive out several milliampere current when LED flashing. EMI issue should be considered. It is a normal way to solve the EMI issue that keeping the two traces far away from other signal trace and adding 470pF capacitor close to each LED diode.

LED0 and LED1 pin are multiplexed as power on strapping pins. If the two pin should be pulled down for power on strapping, the schematic should change to *Figure 15*.

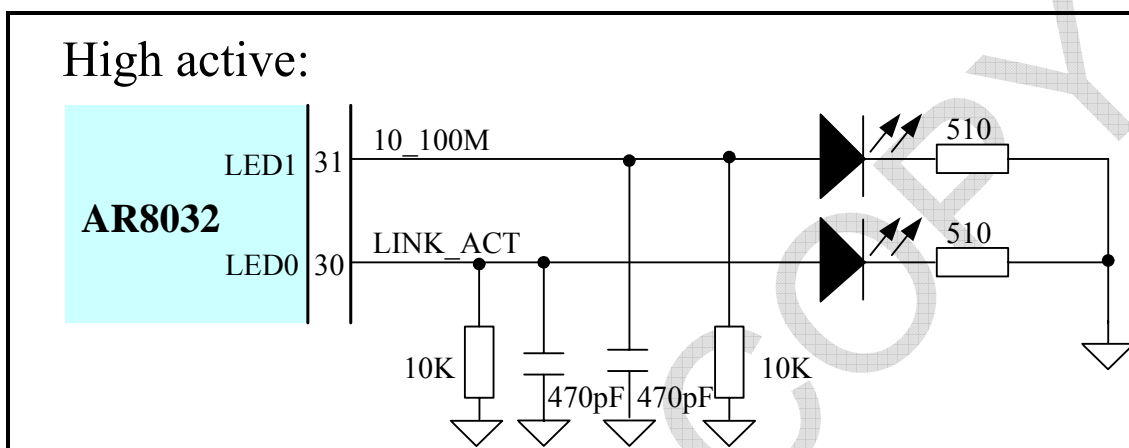


Figure 15: two special LED circuit with pull down resistor

7. System signals

Table 4 is the pinout map and pin description of the system signals.

Table 4: System signal pin map and description

Symbol	Pin	Type	Description
RST#	10	IH, PU	System reset, active low, connect 10k Ω to 2.5V and 0.1 μ F to ground.
XI	9	AI	Crystal oscillator input. 27pF to GND. An external 25/50 MHz clock source with 1.2V swing can inject from this pin when a crystal is not used and the two 27pF caps removed. The 25Mhz clock input is for MII mode, while the 50Mhz clock input is for RMII mode.
XO	8	AO	Crystal oscillator output. 27pF to GND.
REXT	32	AO	External 2.37k Ω 1% to ground to set bias current

7.1 System Reset

AR8032 reset signal needs 1ms low logic level for a valid reset. There are two types of circuits for system reset and shown as *Figure 16*.

- (1) Build a RC charge up circuit for power on reset in which resistor equal 10k Ω to 2.5V and capacitor equal 0.1 μ F, *Figure 16(a)*.
- (2) Connect to system reset signal. The precondition is the system reset must keep low level longer than 1ms when power on, *Figure 16(b)*.
- (3) Connect to CPU system reset signal. The precondition is the system reset must keep low level longer than 1ms when power on, *Figure 16(c)*.

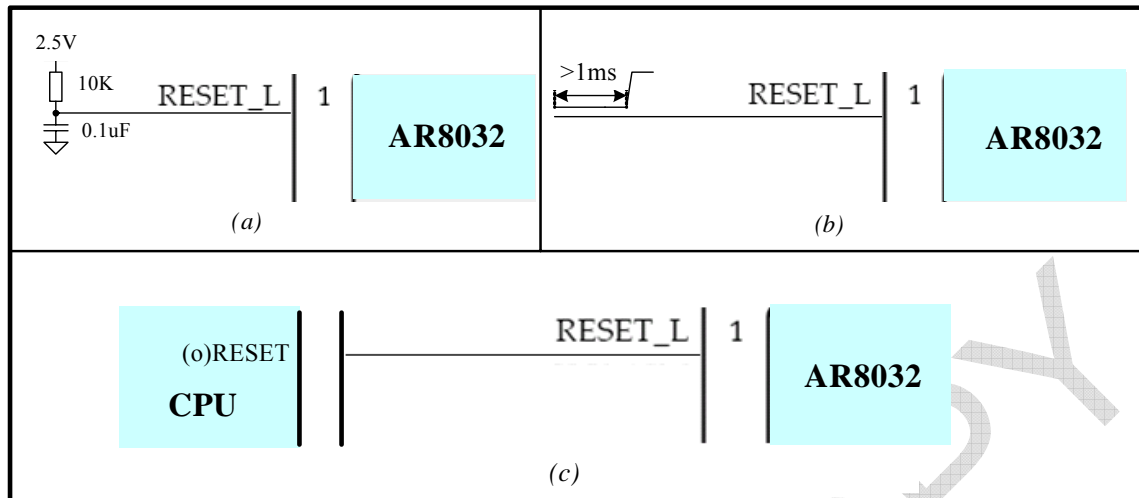


Figure 16: System reset circuit

System reset trace should be far away from other signals (more than 20mils space) for cross talk and keep valid reset signal for system normal running.

7.2 System Clock

The AR8032 supports a low system clock rate of 25MHz which is generated by a crystal. All clock circuits are shown below Figure 17.

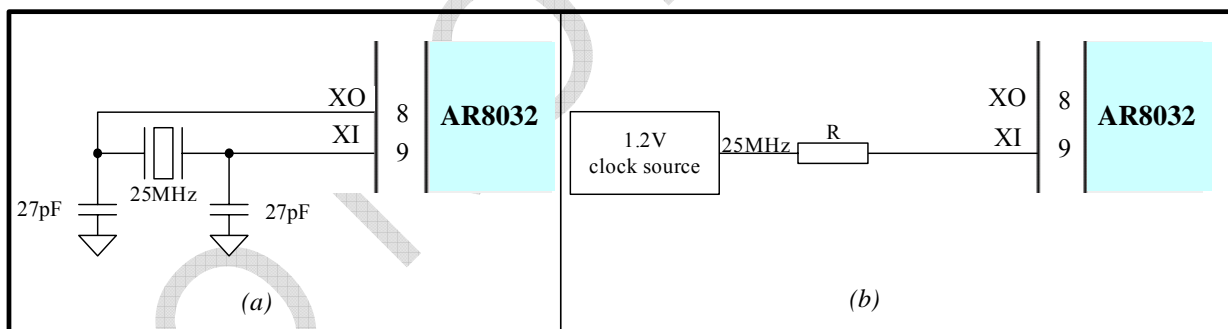


Figure 17: 25MHz clock circuits

When using crystal as Figure 17(a), rules below should be followed:

- (1) The capacitors and crystal should be kept as close to the AR8032 as possible to minimize EMI issues, .
- (2) It is recommended that the crystal accuracy be $\pm 50\text{ppm}$, which will account for crystal manufacturing tolerances, so that the $\pm 100\text{ppm}$ IEEE specification can be met. (For MII interface only)

An external 25MHz clock source with 1.2V swing can be used in place of the crystal, Figure 17(b). This source can be injected to XI with XO floating. If the clock swing is larger than 1.5V, the swing must be decreased. For example,

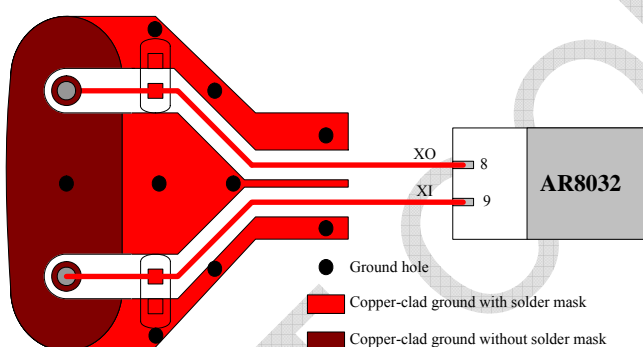
if the clock source is 3.3V swing, we should use the similar method to decrease the clock swing to 1.2V used for RMI interface in Section 5.

The system clock is a critical and sensitive signal. It can cause EMI issues if this part of the circuit is not well thought out during the PCB layout process. *Figure 18* shows an example layout that can minimize EMI issues.

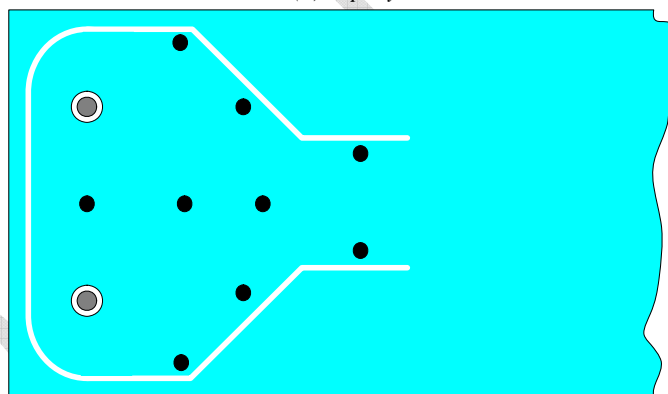
Top layer: Signal
 Internal layer1: Ground
 Internal layer2: Power
 Bottom layer: Signal



(a) layer stack



(b) Top layer



(c) Ground layer

Figure 18: Crystal PCB Layout Example

The crystal in demo circuit above is a through-hole one. If it is a surface-mounted crystal, the layout rule is also compatible. On the ground layer, the split gap should be 20mils. Following these layout rules can reduce EMI issues caused by the crystal.

7.3 REXT

REXT pin is connected with $2.37k\Omega \pm 1\%$ resistance to ground to provide a precise reference voltage for AR8032 internal analog circuitry. The resistor should be placed close to AR8032 and keep the resistor and trace far away from other routing trace (at least 25mils) for a low noise environment, especially for clock trace and MDI interface trace. Around with ground or put the resistor to bottom side is a good choice if clock trace and MDI interface trace are on top layer.

8. Power Supply and Ground

The AR8032 need two power supplies: 2.5V, 1.2V. All of them can be generated by on chip regulator from 3.3V power input. In particular, 1.2V/2.5V on chip regulator doesn't need a PNP transistor. All of power pins, regulator pin and ground pin are listed as following Table 5.

Table 5: Power signal pin map and description

Symbol	Pin	Description
VDD3	2	3.3V power supply
VDD12_REG	1	1.2V regulator output. Several 1uF plus a 0.1uF cap needed to stabilize the output
VDD25_REG	3	2.5V regulator output. Several 1uF ceramic caps needed to stabilize the output. It is for analog, digital I/O and the transformer center taps.
VDD25	17	2.5V I/O power, connect with pin 3, 0.1uF to GND.
GND	E-pad	Exposed ground pad on the back side of the chip, tie to ground

Figure 19 is 3.3V/2.5V/1.2V power supply schematic circuit for commercial version AR8032.

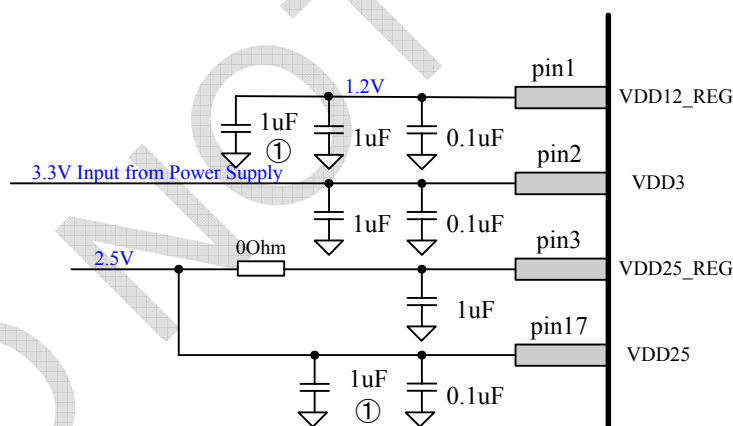


Figure 19: 3.3V/2.5V/1.2V power supply circuit

The capacitors with symbol ① are used for industry version of AR8032

8.1 3.3V Power Supply

Pin2 is 3.3V power supply for internal on chip two regulator power sources. A 1uF ceramic capacitor and 0.1uF capacitor are for decoupling. 2.5V and 1.2V power output are translated by this power supply. When AR8032 is used on motherboard, Auxiliary 3.3V power supply can be used. Auxiliary power is necessary to support wake up from power down states through Ethernet port.

8.2 2.5V Power Supply

2.5V power supply is generated by on chip regulator. The schematic circuit is as shown in *Figure 19*.

2.5V power pins include two parts: a 2.5V Regulator output pin and a 2.5V digital power pin. Pin3 is 2.5V on chip regulator output and is also a 2.5V analog power. 2.5V is also used for transformer centre-tap power supply.

For commercial version of AR8032, one 1uF capacitor is used for stabilize the 2.5V output power at VDD25_REG output side and one 0.1uF capacitor is used for 2.5V input side.

For industry version of AR8032, one 1uF capacitor is used for stabilize the 2.5V output power at VDD25_REG output side and one 1uF plus one 0.1uF capacitors are used for 2.5V input side.

8.3 1.2V Power Supply

This section is used for commercial version AR8032, for industry version please refer to Section 10.

1.2V power supply is generated by on chip regulator. The schematic circuit is as shown in *Figure 19*.

Pin1 is the on chip 1.2V regulator output. For commercial version of AR8032, a 1uF ceramic capacitor and 0.1uF capacitor are needed for voltage stabilization.

For industry version of AR8032, two 1uF ceramic capacitors and 0.1uF capacitor are needed for voltage stabilization.

In PCB layout file, this trace must be far away from other signal trace (at least 20mils space) and as short as possible (less than 1inch and more than 10mils width).

8.4 Power Pin Decoupling

To reduce power noise and EMI, 0.1uF decoupling capacitors are required for every power pin. Capacitors are better placed near the related pins. In general, one 10uF ceramic capacitor and one 0.1uF capacitors are needed to stabilize each regulator.

Decoupling capacitors should be placed as close as possible to the power pins, such that the distance from the IC power pin to the capacitor is less than 200mils.

8.5 Power plane

To simplify design and to make PCB cost effective, all powers can share the same layer. An example layout is shown in *Figure 20*.

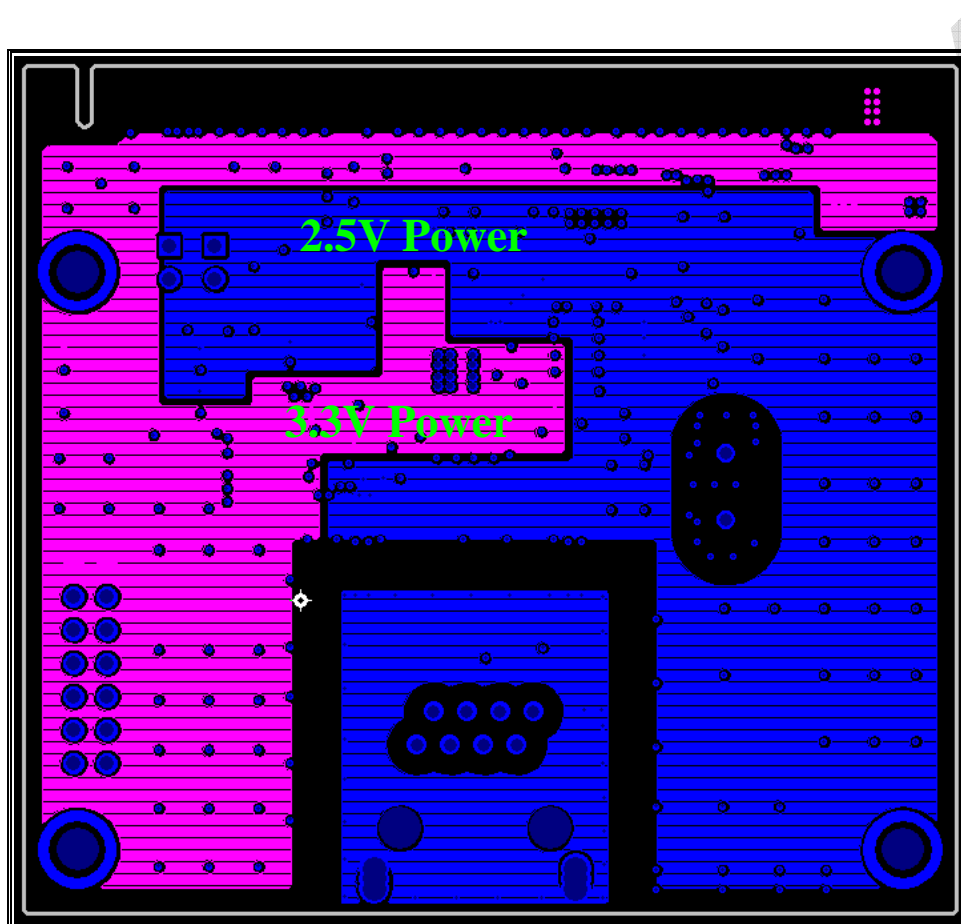


Figure 20: Power plane split

The splitting gap between different planes is 20mils safe space.

8.6 Ground

AR8032 ground pin is the exposed pad on the bottom side of the chip. In PCB layout, this pad ties to system ground directly. At the same time, a majority of hot dissipation implements through this exposed pad.

Figure 21 shows 4×4 vias to ground to increase heat dissipating area and to ensure good ground contact. On top

side, the size of copper-clad ground without solder mask should equal to AR8032 exposed pad.

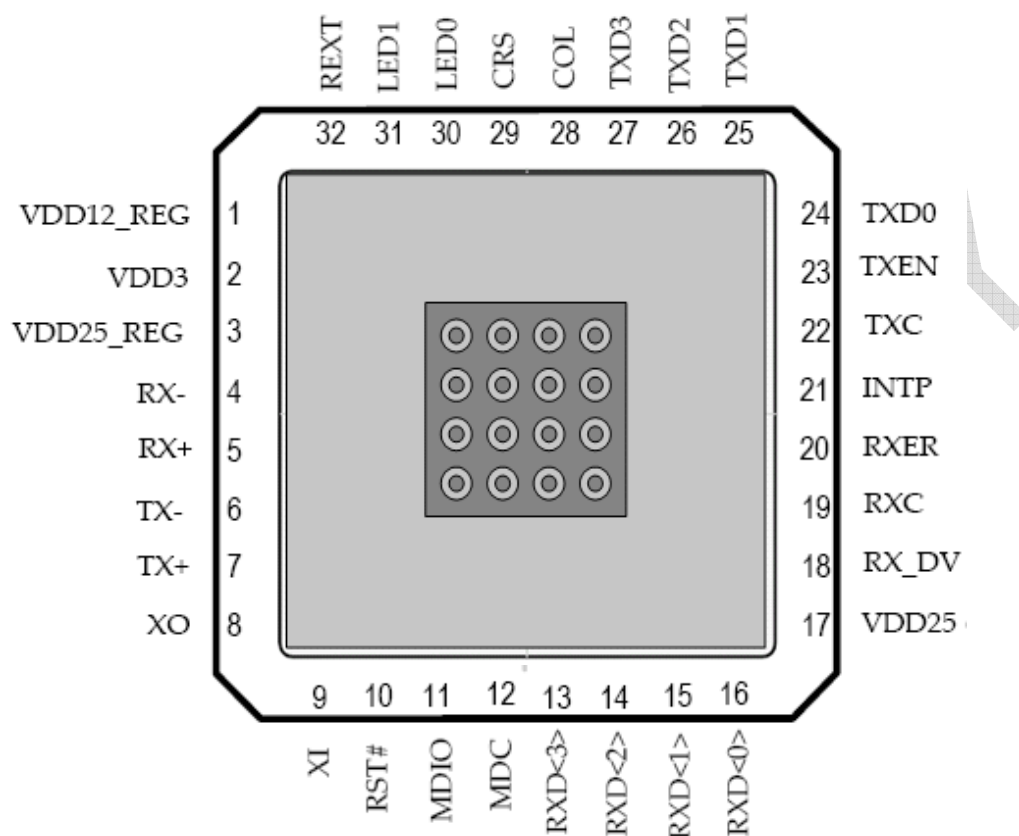


Figure 21: AR8032 ground

There is only one ground for all the power. Separating between Analog and Digital Ground domains is not recommended.

Chassis Ground and System Ground

Figure 22 shows the preferred method for implementing a ground split under the transformer. The capacitor stuffing options (C1 to C2) are used to reduce and filter high frequency emissions. The values of the capacitor stuffing options can be different for each board. Experiments need to be performed to determine which values provide best EMI performance. The value range of cap is from 470pF to 10uF according to bad EMI frequency point.

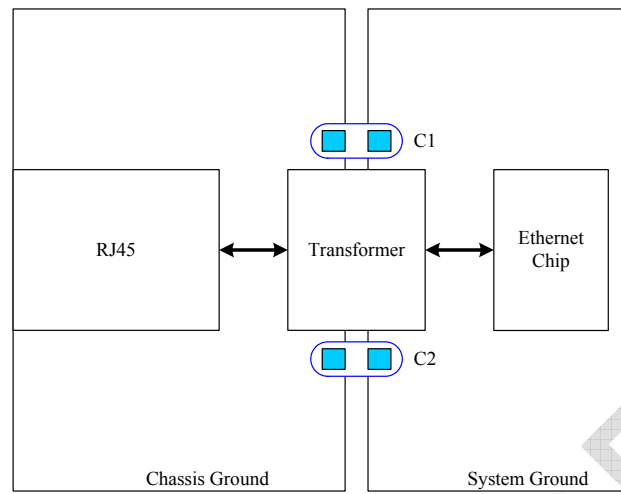


Figure 22: Caps between Chassis Ground and System Ground for EMI

9. Power On Strapping

Power on strapping pins list as following *table 6*.

Table 6: Power on strapping pin map and description

PHY Pin	Pin	PHY Core Config Signal	Descriptions		Default
RXD3	13	PHYADDRESS0	RXD[1:3] set the lower three bits of the physical address. The upper two bits of the physical address default to 001.		1
RXD2	14	PHYADDRESS1			0
RXD1	15	PHYADDRESS2			0
RXD0	16	DUPLEX	0	Half Duplex	1
			1	Full Duplex	
RXDV	18	CONFIG2	CONFIG[2:0] 000 = MII 001 = RMII All other binary combinations are Reserved.		000
CRS	29	CONFIG1			
COL	28	CONFIG0			
RXER	20	ISOLATE	0	Disable	0
			1	Enable	
INTP	21	TEST MODE	0	Test mode	1
			1	Normal operation	
LED0	30	AUTO-NEGOTIATION	0	Disable	1
			1	Enable	
LED1	31	SPEED	0	10 Base-T	1
			1	100 Base-Tx	
RXC	19	POWER DOWN MODE	0	Disable	0
			1	Enable	
TXC	22	En_10ab & En_100ab	0	The AR8032 will be in 10/100M Class AB mode	1
			1	The AR8032 will be in 10/100M Class A mode	

The power-on strapping resistor is 10kΩ for pulling up and pulling down. If pin configuration pulls high, then the resistor should be pulled up to 2.5V.