AT&T Microelectronics

ATTL7543 Line Card Access Switch

Features

- Small size/surface-mount packaging
- Monolithic IC reliability
- Clean, bounce-free switching
- Low, matched ON-resistance
- Built-in current limiting, thermal shutdown, and SLIC protection
- Very low power consumption
- No EMI

Applications

- Central office
- DLC
- PBX

Description

The ATTL7543 Line Card Access Switch (LCAS) is a monolithic integrated circuit that contains ten solid-state switch contacts designed to replace electromechanical relays (EMR) in central office and digital loop carrier analog line-card applications. Through application of appropriate control signals to three logic level inputs, the idle or talk state, power ringing, line test access, SLIC test access, and ringing generator test access states are achievable via the LCAS IC.

The line break switch pair is a linear switch that has exceptionally low ON-resistance and an excellent ON-resistance matching characteristic. The ringing access switch has a breakdown voltage rating >450 V which is sufficiently high enough to prevent breakdown (i.e., passing the transient on to the ringing generator) in the presence of a transient fault condition.

Incorporated into the LCAS is a foldover type SLIC protection circuit that limits the voltage seen by the SLIC and shunts currents to a ground device during a fault condition. Thus, the LCAS eliminates the need for a separate SLIC protection device.

To protect the LCAS from an overvoltage fault condition, use of a secondary protector is required. The secondary protector must limit the voltage applied to the LCAS to $<\pm 250$ V. Use of a foldback or crowbar type secondary protector is recommended. The line break switch pair and access switches (except those connected to the ringing generator) have a current-limit feature that will limit the current through the switch in the presence of a transient fault condition.

Also incorporated into the LCAS is a thermal shutdown circuit that will cause the chip to shutdown (all switches off) when excessive power dissipation, such as what is encountered in the presence of an extended power cross, causes the chip temperature to rise above a given threshold. With the proper design of SLIC circuitry, proper selection of secondary protector, and series resistors, the LCAS will meet appropriate regulatory agency requirements.

The LCAS requires +5 V, battery voltage, and ground to operate. The LCAS device is packaged in a 24-pin plastic DIP (ATTL7543AF/BF) and in a 28-pin, plastic SOG package (ATTL7543AAJ/BAJ).

Pin Information

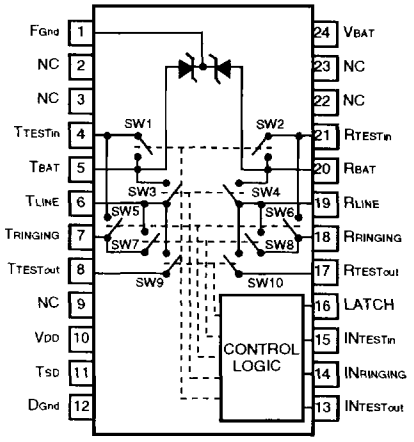


Figure 1. 24-Pin, Plastic DIP

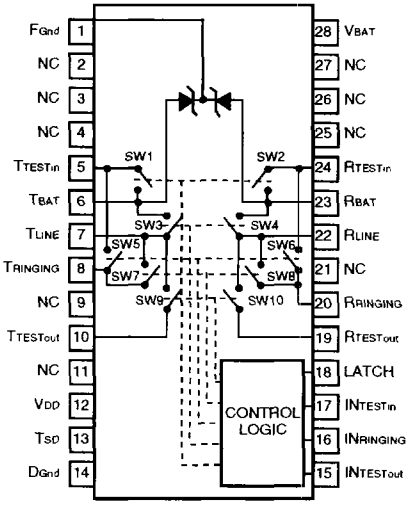


Figure 2. 28-Pin, Plastic SOG

Table 1. Pin Descriptions

DIP	SOG	Symbol	Description	DIP	SOG	Symbol	Description
1	1	FGnd	Fault ground.	24	28	VBAT	Battery voltage.
2	2	NC	No connection.	23	26, 27	NC	No connection.
3	3, 4	NC	No connection.	22	25, 21	NC	No connection.
4	5	TTESTin	Test (in) access on TIP.	21	24	RTESTin	Test (in) access on RING.
5	6	TBAT	Connect to TIP on SLIC side.	20	23	RBAT	Connect to RING on SLIC side.
6	7	TLINE	Connect to TIP on line side.	19	22	RLINE	Connect to RING on line side.
7	8	TRINGING	Connect to return ground for ringing generator.	18	20	RRINGING	Connect to ringing generator.
8	10	TTESTout	Test (out) access on TIP.	17	19	RTESTout	Test (out) access on RING.
9	9, 11	NC	No connection.	16	18	LATCH	Data input control, active-high, transparent low.
10	12	VDD	+5 V supply.	15	17	INTESTin	Logic level switch input control.
11	13	TSD	Temperature shutdown output flag will read +5 V when the device is in its operational mode and 0 V in the thermal shutdown mode. To disable the thermal shutdown mechanism, tie this pin to +5 V.	14	16	INRINGING	Logic level switch input control.
12	14	DGnd	Digital ground.	13	15	INTESTout	Logic level switch input control.

Electrical Characteristics

T_A –40 °C to +85 °C, unless otherwise specified.

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Table 2. Power Supply Specifications

Parameter	Power Supply, V_{DD}	Power Supply, V_{BAT}
Nominal Voltage	+5 V	–48 V/–60 V*
Voltage Tolerance	±0.5 V	±20%

* Choice of SLIC protection circuit trigger voltage is determined by the maximum voltage of V_{BAT}. See SLIC Protection Circuit section for details.

Table 3. Test In Switch, 1 and 2

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Off-state Leakage Current/Min Breakdown Voltage	Vswitch (differential) = –320 V to Gnd Vswitch (differential) = –60 V to +260 V	Iswitch	—	—	1	µA
ON Resistance	Iswitch (on) = ±5 mA, ±10 mA	Δ V_{on}	—	30*	50	Ω
Isolation	Vswitch (both poles) = ±320 V Logic Inputs = GND	Iswitch	—	—	1	µA
dv/dt Sensitivity†	—	—	—	200	—	V/µs

* At 25 °C.

† Applied voltage is 100 Vpp square wave at 100 Hz.

Table 4. Break Switch, 3 and 4

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Off-state Leakage Current	Vswitch (differential) = –320 V to Gnd Vswitch (differential) = –60 V to +260 V	Iswitch	—	—	1	µA
ON Resistance	Iswitch (on) = ±10 mA, ±40 mA	Δ V_{on}	—	15 *	28	Ω
ON-resistance Match	Per ON-resistance Test Condition of SW3, SW4	Magnitude R_{ON} SW3—R_{ON} SW4	—	—	1	Ω
Current Limit	Vswitch (on) = ±10 V	Iswitch	80	—	220	mA
Isolation	Vswitch (both poles) = ±320 V Logic Inputs = GND	Iswitch	—	—	1	µA
dv/dt Sensitivity*	—	—	—	200	—	V/µs

* At 25 °C.

† Applied voltage is 100 Vpp square wave at 100 Hz.

Table 5. Ringing Test Return Switch 5

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Off-state Leakage Current	Vswitch (differential) = +60 V to –260 V Vswitch (differential) = –60 V to +260 V	Iswitch	—	—	1	µA
ON Resistance	Iswitch (on) = 5 mA, 10 mA	Δ V_{on}	—	50*	100	Ω
Isolation	Vswitch = ±320 V Logic Inputs = GND	Iswitch	—	—	1	µA
dv/dt Sensitivity†	—	—	—	200	—	V/µs

* At 25 °C.

† Applied voltage is 100 Vpp square wave at 100 Hz.

Electrical Characteristics (continued)

Table 6. Ringing Test Switch 6

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Off-state Leakage Current	Vswitch (differential) = +60 V to −190 V Vswitch (differential) = −60 V to +190 V	Iswitch	—	—	1	µA
ON Resistance	Iswitch (on) = ±70 mA, ±80 mA	Δ Von	—	—	20	Ω
On Voltage (Vos)	Vswitch (on) = ±1.5 V	Iswitch	—	—	1	mA
Isolation	Vswitch = ±320 V Logic Inputs = GND	Iswitch	—	—	1	µA
Release Current	—	—	100	—	500	µA
dv/dt Sensitivity*	—	—	—	200	—	V/µs

* Applied voltage is 100 Vpp square wave at 100 Hz.

Table 7. Ringing Return Switch 7

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Off-state Leakage Current	Vswitch (differential) = −320 V to Gnd Vswitch (differential) = −60 V to +260 V	Iswitch	—	—	1	µA
ON Resistance	Iswitch (on) = ±5 mA, ±10 mA	Δ Von	—	50*	100	Ω
Current Limit	Vswitch (on) = ±50 V	Iswitch	200	—	400	mA
Isolation	Vswitch = ±320 V Logic Inputs = GND	Iswitch	—	—	1	µA
dv/dt Sensitivity†	—	—	—	200	—	V/µs

* At 25 °C.

† Applied voltage is 100 Vpp square wave at 100 Hz.

Table 8. Ringing Switch 8

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Off-state Leakage Current	Vswitch (differential) = +260 V to −190 V Vswitch (differential) = −260 V to +190 V	Iswitch	—	—	1	µA
ON Resistance	Iswitch (on) = ±70 mA, ±80 mA	Δ Von	—	—	10	Ω
ON Voltage	Iswitch (on) = ±1 mA	Vos	—	—	3	V
On Voltage (Vos)	Iswitch (on) = ±1 mA	Vos	—	—	3	V
Isolation	Vswitch = ±320 V Logic Inputs = GND	Iswitch	—	—	1	µA
Surge Current	—	—	—	—	2	A
Release Current	—	—	100	—	500	µA
dv/dt Sensitivity †	—	—	—	200	—	V/µs

* Applied voltage is 100 Vpp square wave at 100 Hz.

Electrical Characteristics (continued)

Table 9. Test Out Switch, 9 & 10

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Off-state Leakage Current	Vswitch (differential) = –320 V to GND Vswitch (differential) = –60 V to +260 V	Iswitch	—	—	1	µA
ON Resistance	Iswitch (on) = ±5 mA to 10 mA	Δ V_{on}	—	30*	65	Ω
Current Limit	Vswitch (on) = ±50 V	Iswitch	100	—	220	mA
Isolation	Vswitch (both poles) = ±320 V Logic Inputs = GND	Iswitch	—	—	1	µA
dv/dt Sensitivity†	—	—	—	200	—	V/µs

* At 25 °C.

† Applied voltage is 100 Vpp square wave at 100 Hz.

Table 10. Additional Electrical Characteristics

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Digital Input Characteristics: Input Low Voltage	—	—	—	—	1.5	V
Input High Voltage	—	—	3.5	—	—	V
Input Leakage Current (High)	V_{DD} = 5.5 V, V_{BAT} = –58 V, Vlogicin = 5 V	Ilogicin	—	—	1	µA
Input Leakage Current (Low)	V_{DD} = 5.5 V, V_{BAT} = –58 V, Vlogicin = 0 V	Ilogicin	—	—	1	µA
Power Requirements: Power Dissipation	V_{DD} = 5 V, V_{BAT} = –48 V, Idle/Talk State or All Off State Ringing State or Access State	I_{DD}, I_{BAT} I_{DD}	— —	1.7 4	2 10	mW mW
V_{DD} Current	V_{DD} = 5 V, Idle/Talk State or All Off State Ringing State or Access State	I_{DD} I_{DD}	— —	— 750	300 —	µA µA
V_{BAT} Current	V_{BAT} = –48 V, Idle/Talk State or All Off State Ringing State or Access State	I_{BAT} I_{BAT}	— —	4 4	— —	µA µA
Digital Input Characteristics: Input Low Voltage	—	—	—	—	1.5	V
Input High Voltage	—	—	3.5	—	—	V
Input Leakage Current (High)	V_{DD} = 5.5 V, V_{BAT} = –58 V, Vlogicin = 5 V	Ilogicin	—	—	1	µA
Input Leakage Current (Low)	V_{DD} = 5.5 V, V_{BAT} = –58 V, Vlogicin = 0 V	Ilogicin	—	—	1	µA
Temperature Shutdown Requirements:* Shutdown Activation Temperature	—	—	110	125	150	°C
Shutdown Circuit Hysteresis	—	—	10	—	25	°C

* Temperature shutdown flag (TSD) will be high during normal operation and low during temperature shutdown state.

Zero Cross Current Turn Off

The ring access switch (SW8) and the ringing test switch (SW6) are designed to turn off on a zero current cross. These switches require a current zero cross at the battery voltage to turn off. Switch 8 (SW8) and switch 6 (SW6) will remain in the on state (regardless of logic input) until a current zero cross. Therefore, to ensure proper operation, switch 8 and switch 6 should be connected to the ringing generator (via proper impedance).

SLIC Protection Circuit

The SLIC protection circuit, shown in Figure 3, as two zener diodes, is included in the ATTL7543 LCAS IC device to protect the SLIC from fault-induced overvoltage situations. With this feature, the only secondary protection required on the line card is the 210 V—250 V protector on the loop side of the solid-state switch. The SLIC is protected by a combination of the current limit in the SLIC break switches (SW3 and SW4) and the SLIC protection circuit.

In reality, this circuit consists of MOSFET transistors that are turned on when the voltage at the SLIC is more negative than the battery or more negative than an internal zener diode reference (clamp voltage). For positive fault conditions, the protection circuit will conduct when the SLIC exceeds one diode drop. The characteristics of the protection circuit are shown in Figures 4 and 5.

Two different clamp voltages are available for the ATTL7543 LCAS IC device. The first alpha character after the numerical device identifier designates the clamp voltage version. The A character designate is intended for a battery voltage of –48 V ± 20%, and the B character designate is intended for battery voltages of –60 V ± 20%. Tables 6 and 7 give the specifications for the leakage at the maximum battery voltage (–58 V or –72 V), the voltage at which 1 mA is conducted, and the voltage at which the clamp circuit conducts the maximum dc current that can be carried by switches 3 or 4 (I_{LIMIT} SW3, SW4).

The information shown in Tables 11 and 12 is referenced in Figures 4 and 5. Compilation of this data was over the full temperature range (–40 °C to + 85 °C).

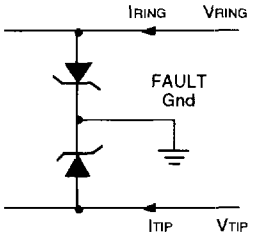


Figure 3. SLIC Protection Circuit

SLIC Protection Circuit (continued)

Table 11. SLIC Protection Circuitry Options (ATTL7543AF/AAJ)

Apply	Condition	Figure	Measure			
			Parameter	Min	Max	Unit
$R_{BAT} = V_{BAT}$ $T_{BAT} = V_{BAT}$	$V_{BAT} = -58$ V	4	$I_{FAULTGROUND}$	—	1	µA
$I_{FAULTGROUND} = -1$ mA	$V_{BAT} = -58$ V	4	T_{BAT} R_{BAT}	$V_{BAT} + (-4$ V)	—	V
$I_{FAULTGROUND} = -I_{Limit}$ SW1, SW2	$V_{BAT} = -58$ V	4	T_{BAT} R_{BAT}	$V_{BAT} + (-14$ V)	—	V
$I_{FAULTGROUND} = +I_{Limit}$ SW1, SW2	$V_{BAT} = -58$ V	4	T_{BAT} R_{BAT}	—	3	V
$T_{BAT} = -60$ V (V1 Fig 5) $R_{BAT} = -60$ V (V1 Fig 5)	V_{BAT} = No Connection	5	$I_{FAULTGROUND}$	1	1	µA
$I_{FAULTGROUND} = -1$ mA	V_{BAT} = No Connection	5	T_{BAT} (V2 Fig 5) R_{BAT} (V2 Fig 5)	–70	—	V
$I_{FAULTGROUND} = +I_{Limit}$ SW3, SW4	V_{BAT} = No Connection	5	—	—	3	V

Table 12. SLIC Protection Circuitry Options (ATTL7543BF/BAJ)

Apply	Condition	Figure	Measure			
			Parameter	Min	Max	Unit
$R_{BAT} = V_{BAT}$ $T_{BAT} = V_{BAT}$	$V_{BAT} = -72$ V	4	$I_{FAULTGROUND}$	—	1	µA
$I_{FAULTGROUND} = -1$ mA	$V_{BAT} = -72$ V	4	T_{BAT} R_{BAT}	$V_{BAT} + (-4$ V)	—	V
$I_{FAULTGROUND} = -I_{Limit}$ SW1, SW2	$V_{BAT} = -72$ V	4	T_{BAT} R_{BAT}	$V_{BAT} + (-14$ V)	—	V
$I_{FAULTGROUND} = +I_{Limit}$ SW1, SW2	$V_{BAT} = -72$ V	4	T_{BAT} R_{BAT}	—	3	V
$T_{BAT} = -77$ V (V1 Fig 5) $R_{BAT} = -77$ V (V1 Fig 5)	V_{BAT} = No Connection	5	$I_{FAULTGROUND}$	1	1	µA
$I_{FAULTGROUND} = -1$ mA	V_{BAT} = No Connection	5	T_{BAT} (V2 Fig 5) R_{BAT} (V2 Fig 5)	–87	—	V
$I_{FAULTGROUND} = +I_{Limit}$ SW3, SW4	V_{BAT} = No Connection	5	—	—	3	V

Typical Performance Characteristics

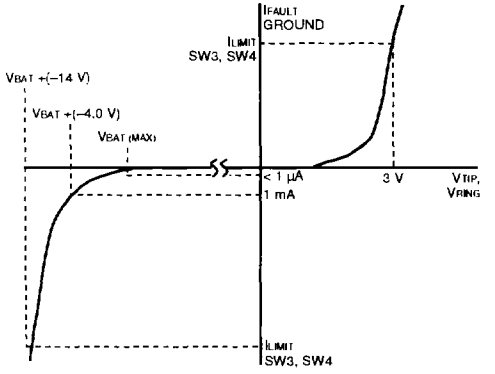


Figure 4. Characteristics of ATTL7543 (V_{BAT} Present)

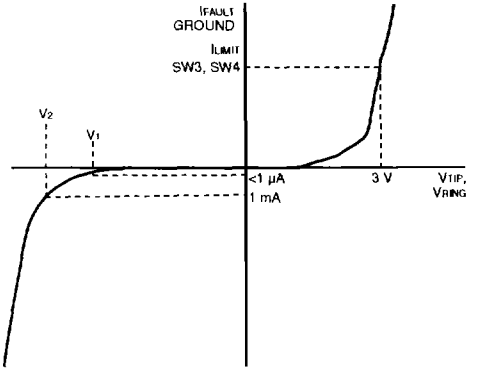


Figure 5. Characteristics of ATTL7543 (V_{BAT} Not Present)

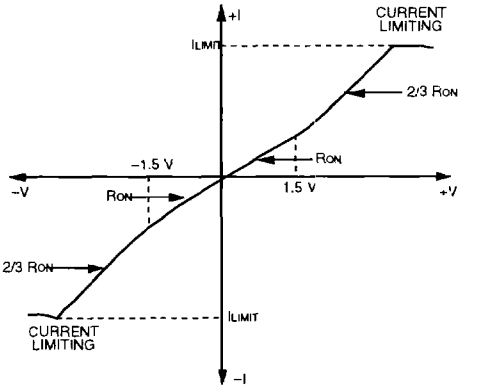


Figure 6. Switch 1—5, 7, 9, 10

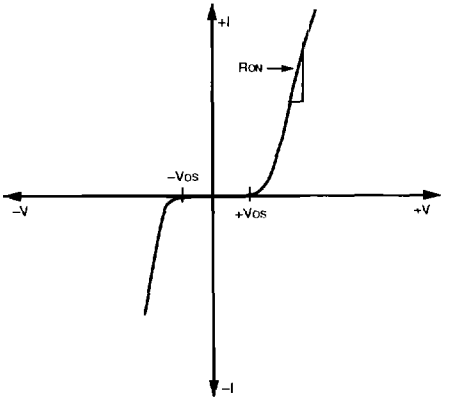


Figure 7. Switch 6, 8

Application

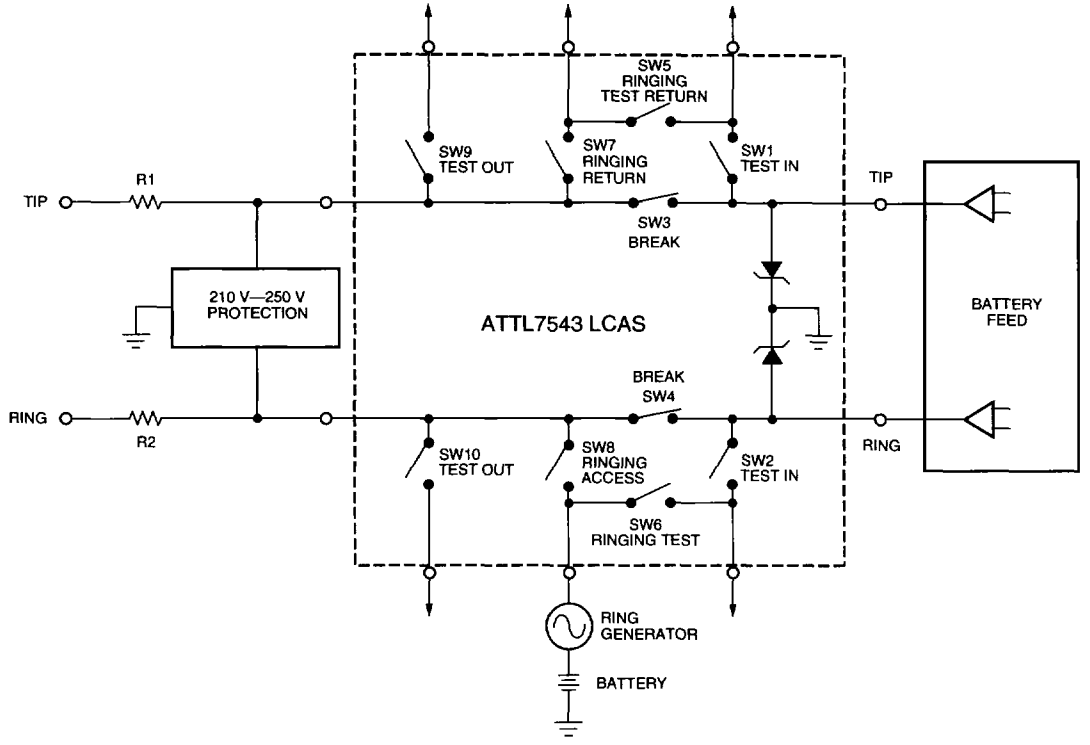


Figure 8. Typical LCAS Application, Idle or Talk State Shown

Table 13. Truth Table

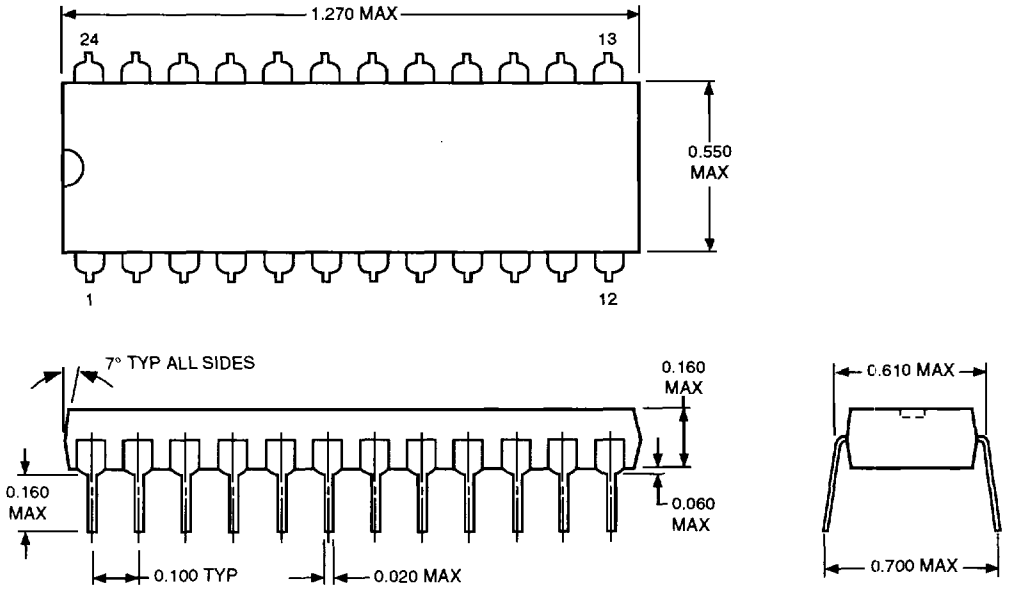
Input			Switches					State Description
Ring	Test In	Test Out	Test In SW1/2	Break SW3/4	Ringing Test SW5/6	Ringing SW7/8	Test Out SW9/10	
Low	Low	Low	Open	Closed	Open	Open	Open	Idle or talking state.
Low	Low	High	Open	Open	Open	Open	Closed	Line test state
Low	High	Low	Closed	Open	Open	Open	Open	SLIC test state.
High	Low	Low	Open	Open	Open	Closed	Open	Power ringing state.
High	High	Low	Open	Open	Closed	Open	Open	Ringing generator test state.*
Low	High	High	Closed	Open	Open	Open	Closed	Simultaneous line test and SLIC test state.
High	Low	High	Open	Open	Open	Open	Open	All off.
High	High	High	Open	Open	Open	Open	Open	All off.

* Power ringing appears at test in node.

Outline Drawings

Dimensions are in inches.

24-Pin, Plastic DIP



Outline Drawings

Dimensions are in inches and (millimeters).

28-Pin, Plastic SOG